Growth and electrical characterization of thin film silicon on MG-Si for solar cell applications

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by

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Abstract

Thin films of silicon for solar cell applications were grown by liquid phase epitaxy (LPE). The films were grown on semi-insulating single-crystalline silicon, p-type single-crystalline silicon and metallurgical grade silicon (MG-Si). MG-Si substrates have higher impurity concentrations than traditional electronic grade silicon and are used as low-cost alternatives to single crystalline substrates. p-n junctions were prepared by growing n-type silicon on p-type MG-Si substrates. The as-grown samples were hydrogenated to improve their electrical quality. Electrical characterization along with a morphology study was made on the grown samples. It was demonstrated that it is possible to produce a low-cost solar cell using metallurgical grade silicon substrates. However, hydrogenation is essential to achieve the desired electrical properties.

Úrdráttur

Þunnar kísilhúðir fyrir notkun í sólarhlöð voru ræktaðar úr vökvafasa með LPE tækni. Húðir voru ræktaðar á hálfeingangrandi einrkristallaðan kísil, p-leiðandi einkristallaðan kísil og MG-kísil. MG-kísil undirlög innihalda hærri styrkleika af óhreinindum en kísill sem notaður er í hálfleiðaraiðnaði. Þau eru því ódýr valkostur við einkristölluð undirlög. p-n samskeyti voru útbúin með ræktun n-leiðandi kísils á p-leiðandi MG-kísil undirlög. Ræktuðu sýnin voru vetnisíbætt til að bæta rafeiginleika þeirra. Rafeiginleikar og yfirborðshrjúfleiki voru mældir fyrir ræktuðu sýnin. Sýnt var fram á að MG-kísil undirlög eru mögulegur kostur í framleiðslu á ódýrum sólarhlöðum. Hinsvegar er vetnisíbæting nauðsynlegt skref til að fá fram æskilega rafeiginleika.

Contents

Chapter 1

Introduction

In the year 2006, 1.8×10^{13} kWh of electrical energy were consumed in the world (E.I.A, 2009). The consumption had increased on the average 3.14% per year over the past two decades. A vast majority of the energy or about two thirds was produced by burning fossil fuels. The interest in renewable energy sources, one of which is solar energy, is continuously growing. Solar energy is one of the most abundant natural sources of energy available to mankind. It can be utilized with photovoltaic devices which can be fabricated from various materials and with various methods. Photovoltaic devices, often referred to as solar cells, convert solar energy directly into electricity. A semiconductor with an appropriate bandgap is used to absorb the photons from the sunlight and generate free charge carriers, electrons and holes. Additionally a mechanism, such as a p-n junction is needed to separate the charge carriers which allows an electric current to flow and be utilized. Solar cells are connected together to form modules to increase the output voltage and current and thus the available power.

The use of solar cells as an energy source/supply is relatively low at this time

or around 0.03% of the global energy production in the year 2006 (E.I.A, 2009). It is expected that this number will rise rapidly in the coming years. The development of solar cells is rapid with continually increasing performance and reduced cost (Swanson, 2007). Currently, photovoltaics is one of the fastest growing energy sectors with 40-50% annual growth during the past five years (Green, 2007; Butler, 2008; Service, 2008). The growth of the photovoltaics industry is mainly driven by silicon based solar cells, in particular poly-crystalline silicon (Braga et al., 2008). Electricity produced from solar cells still costs about five times more than electricity produced with coal, but economics of scale are expected to close the gap by mid next decade (Shaheen et al., 2005; Swanson, 2007; Service, 2008). For photovoltaic technology to compete economically with conventional means of producing electricity the cost of module production has to be reduced to USD 0.33/Watt with module efficiency of roughly 15% (Catchpole et al., 2001). For comparison, the production cost of a module in the year 2007 was USD 3–4/Watt (Slaoui and Collins, 2007).

Solar cells can be made from various types of semiconducting materials, which can be amorphous, polycrystalline or single-crystalline. The semiconductors include silicon, III–V semiconductors such as GaAs and InP and the chalcopyrite compound copper indium gallium diselenide (CIGS) and CdTe. In addition, organic materials, including polymers, have gained attention lately. An in-depth discussion about solar cell materials is given in chapter 2.3. Silicon solar cells remain the dominant technology in the market due to the natural abundance of silicon, its high reliability, ease of processing and high efficiency. Currently 94% of all produced solar cells are made of silicon, whereof 38% is single-crystalline, 49% is poly-crystalline, 4% is amorphous and 3% is silicon ribbons (Miles et al., 2007).

Solar grade silicon wafers are produced by costly silicon purification ingot

growth and dicing process. Roughly half of the cost of a crystalline silicon solar module lies in the cost of the silicon itself (McCann et al., 2001). This has led to extensive research on thin film silicon solar cells. In particular, thin film silicon solar cells fabricated on low cost substrates are an attractive option for the market. At present silicon thin film modules are mainly based on amorphous silicon, either in a multijunction or multiple junction configuration (Green, 2007). However, there is currently active research on the growth of crystalline silicon thin films for solar cell applications (Bergmann, 1999).

Epitaxial layers of silicon have been grown on a single-crystalline Si substrate (Majumdar et al., 2003; Blakers et al., 1992; Zheng et al., 1996). In order to reduce the amount of silicon used, and thus the cost, thin films have been grown on cast metallurgical-grade (MG) poly-crystalline silicon substrate by liquid phase epitaxy (LPE) (Ciszek et al., 1993). Yamamoto et al. (1999) and Catchpole et al. (2001) discussed growth of thin film poly-Si films on glass substrates at low temperatures. Other developments of new silicon based structures for solar cell applications include low cost mechanically flexible solar cells made from ultra thin single-crystalline silicon (Yoon et al., 2008; Fan and Javey, 2008) and growth of silicon nanowire arrays (Peng et al., 2005; Garnett and Yang, 2008). Recently the application of nanodefect engineering to reduce the electrical activity of metallic impurities of a dirty silicon has been demonstrated (Buonassisi et al., 2005) which is one further attempt to eliminate the dependence on high-quality silicon feedstock. The motivation for this current work is mainly the need for inexpensive raw materials for solar cell production. By using metallurgical grade silicon as a substrate for p-n junction solar cells, the total production cost can be reduced and thereby lowering the cost per module unit area. However, it is clear that the efficiency of solar cells is being traded for cost.

Here we grow silicon thin films on crystalline silicon and metallurgical grade silicon by LPE. Subsequently the as grown samples are exposed to hydrogen plasma in order to passivate defects. The quality of the grown films is assessed by electrical characterization along with a morphology study. The historical developments of silicon solar cells and the production methods applied to manufacture silicon solar cells are reviewed in chapter 2. Chapter 2 also discusses the characteristic parameters used to describe solar cells. Chapter 3 discusses the technology behind LPE growth as well as the methods used to characterize the grown films. The growth of thin film silicon, and their electrical, structural and morphological properties are discussed in chapter 4.

Chapter 2

Silicon solar cells

Solar cells are mainly made of semiconductors. Silicon is the most commonly used material because it exists in large quantities as silicon dioxide (sand, quartz, silica), it is inexpensive compared to other semiconducting materials and is non-toxic. However, a large disadvantage is that silicon has an indirect bandgap which results in a lower photon absorption when compared with direct bandgap materials. A discussion of other materials used for solar cells is in given in chapter 2.3.

A conventional solar cell is fabricated from inorganic semiconducting materials such as crystalline silicon (c-Si). Traditionally, the silicon is purified to a high level, grown into a single crystal ingot, sliced into wafers and then doped to form a p-n junction. Solar cells can be considered a modular power source. A typical cell with a surface area of $1\,\mathrm{cm}^2$ produces less than half a watt of power at its peak maximum. Several of these cells are connected in serial or parallel and encapsulated to form a module. Additional devices are used for voltage inversion and regulation. Figure 2.1 shows a poly-crystalline silicon substrate along with a solar module with antireflection coatings and electrical connections. Currently the production of solar

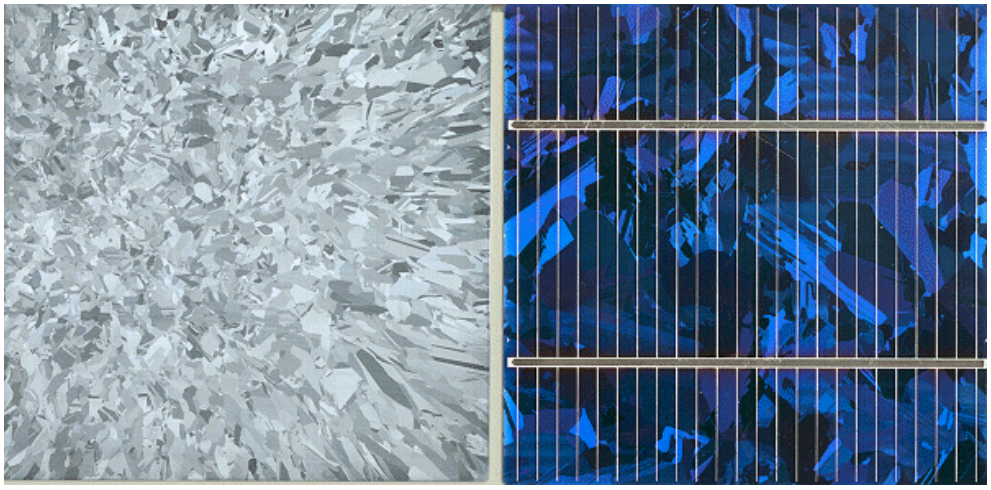


Figure 2.1: On the left is a poly crystalline silicon substrate and on the right is a poly-crystalline silicon solar cell with antireflection coatings and a bus bar.

cells is dominated by the use of single-crystalline and poly-crystalline silicon modules which account for 94% of the market (Miles et al., 2007). These devices are based on silicon wafers and are commonly being referred to as the first generation (I) of photovoltaics technology (Green, 2002, 2003). The first generation cells are single junction cells that have a maximum theoretical power conversion efficiency limit of 29% which occurs at a bandgap of 1.5 eV (Stone, 1993).

The second generation (II) technologies are based on thin films that do not require the use of silicon wafers as a substrate, and thus require much less silicon as compared to the first generation cells, which leads to a significant cost reduction. The aim of the II generation cells is thus to lower the production costs of current cells often by introducing new materials and substrates (Green, 2003). The objective by the third generation (III) solar cells is to improve the electrical efficiency of the second generation cells and to lower the production costs. The third generation technologies are often separated into two categories. The first, IIIa, are novel techniques that are developed to achieve very high efficiencies. The energy conversion

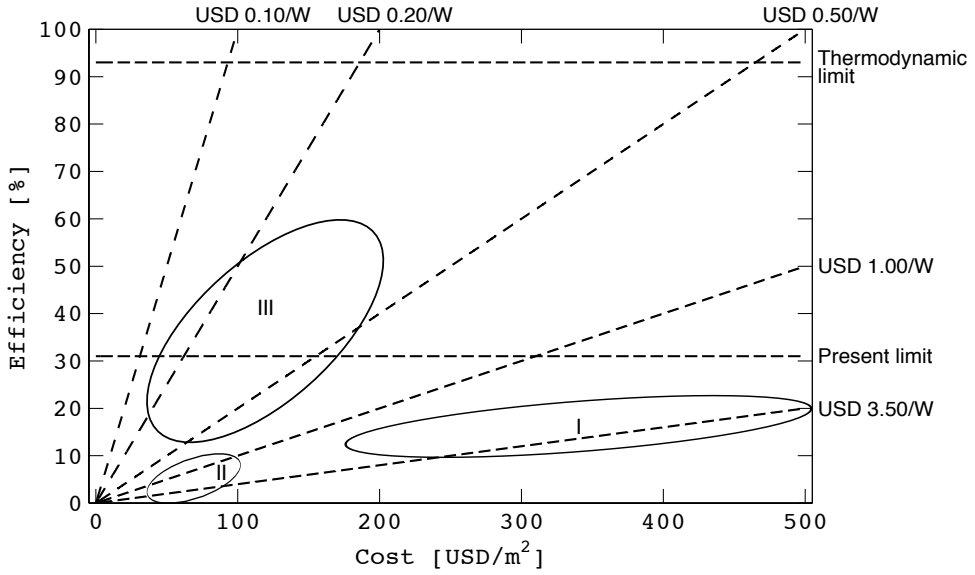


Figure 2.2: Cost - efficiency analysis for the three generation of solar cells. The cost is in year 2003 US dollars. Redrawn from Green (2003).

can at least double and approach the thermodynamic limit of 93% (Green, 2003). The goal of the second category of third generation devices, IIIb, is to reach moderate efficiencies at reasonable cost. Figure 2.2 shows an cost-efficiency analysis for the three generations of photovoltaics technology. Shown in the graph are possible production costs per unit cell area for each solar cell generation and the respective efficiency range (Green, 2003). The work discussed here falls under second generation technology.

2.1 Solar energy

For an accurate comparison of the efficiency of solar cells at different locations, a standard reference spectrum is used for radiation outside the earth's atmosphere and at the earth's surface. For photons to reach the surface of the earth, they must pass through the earth's atmosphere. The length of the path depends on the relative

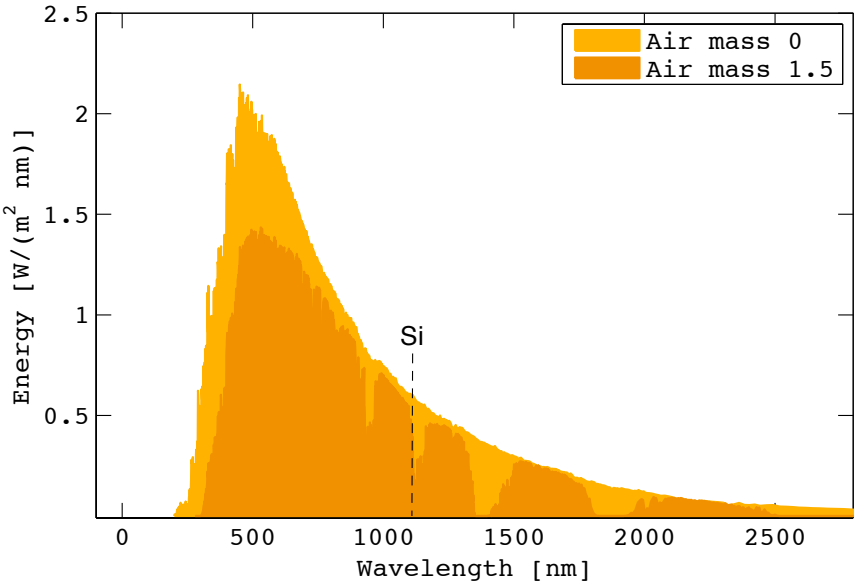


Figure 2.3: The AM0 and AM1.5 solar spectrum (NREL, 2008). The bandgap energy of silicon is marked in as a reference.

position of the sun and the observer. The air mass value is a measure of the air mass that the solar radiation has to travel through. Air mass zero (AM0) represents radiation outside of the earth's atmosphere and is defined to be equal to the solar constant, which is referred to as the total incoming solar electromagnetic radiation per unit area. The solar constant is equal to 1366.1 W/m^2 (it fluctuates with the distance between the earth and sun). The standard conditions for comparing solar cells is the AM1.5 spectrum and refers to when the sun is at 48.19° above horizon giving a power density of 1000 W/m^2. The AM0 and AM1.5 spectrums can be seen in figure 2.3. The standard reference temperature used when measuring the efficiency of solar cells and other relevant parameters is 25° C (Green et al., 2009). A significant part of the incoming radiation is reflected off the surface of the solar cell. For silicon solar cells, this is approximately 30% of the incident light in the spectral range where silicon is photosensitive (Aroutiounian et al., 2004). Antireflection

coatings are added to the surface to minimize the amount of photons that are reflected off the surface. McCann et al. (2001) discusses surface texturization in order to increase the optical confinement. This is often done chemically by wet etching. If care is taken to maximize the optical confinement, conversion efficiency up to 17% can be achieved with active layer thicknesses as low as 1μm (Brendel and Scholten, 1999).

2.2 Historical overview and development

The first practical solar cell was developed at Bell laboratories in 1954 (Chapin et al., 1954). This first solar cell was a p-n junction solar cell in which a thin layer of p-type silicon was grown on an n-type silicon substrate. It had an efficiency of 6%. Since then, the production cost of solar cells has decreased continuously and the performance increased. In 1979 the module cost was USD 32/Watt and by 2002

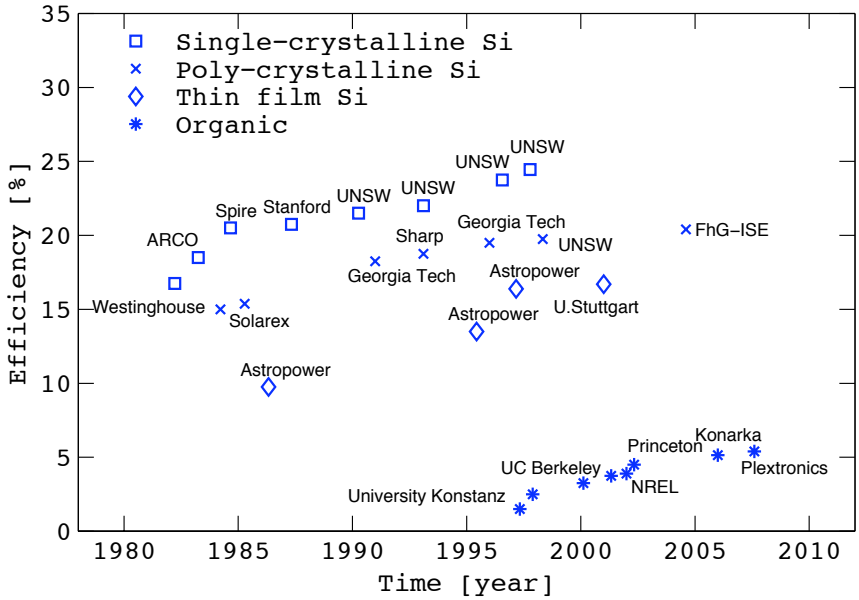


Figure 2.4: Record efficiencies of various types of solar cells (Green et al., 2009).

the module cost had decreased dramatically to USD 3.10/Watt (Swanson, 2007). As of 2007, the best single-crystalline silicon solar cells have reached an efficiency of 25.0% (Green et al., 2009) which is not far from the theoretical maximum value of 29%. An overview of the progress in efficiencies of those types of solar cells over the past several decades can be seen graphically in figure 2.4. Pictured there are the highest efficiency values measured for laboratory solar cells for various types of silicon solar cells as well as organic polymer solar cells. For comparison, the efficiency of commercially available solar cells is in the range of 10–15%. It can be seen that the efficiency is highest for single-crystalline Si solar cells, but lower for poly-crystalline silicon due to effects of grain boundaries on current transport. It is also shown that the efficiency of thin film Si is lower than for single-crystalline Si. However, the efficiency of thin films is higher with respect to the amount of silicon used. Table 2.1 gives an overview of the highest efficiencies achieved, open-circuit voltage and current density for various types of solar cells. A further discussion about efficiency and how it is defined is given in chapter 2.5.1.

Table 2.1: Highest confirmed data measured under AM1.5 spectrum conditions at 25°C (Green et al., 2009).

Type	Efficiency [%]	Area[a] [cm^2]	V_{oc} [V]	J_{sc} [mA/cm^2]
Silicon				
Si (crystalline)	25.0 ± 0.5	4.00 (da)	0.705	42.7
Si (multi-crystalline)	20.4 ± 0.5	1.002 (ap)	0.664	38.0
Si (thin film)	16.7 ± 0.4	4.017 (ap)	0.645	33.0
Si (amorphous)	9.5 ± 0.3	1.070 (ap)	0.859	17.5
III-V				
GaAs (crystalline)	26.1 ± 0.8	0.998 (ap)	1.038	29.7
GaAs (thin film)	26.1 ± 0.8	1.001 (ap)	1.045	84.6
InP (crystalline)	22.1 ± 0.7	4.02 (at)	0.878	29.5
Thin film chalcogenide				
CIGS (cell)	19.4 ± 0.6	0.994 (ap)	0.716	33.7
Organic				
Organic polymer	5.15 ± 0.3	1.021 (ap)	0.876	9.4

[a] : (ap) = aperture area, (t) = total area, (da) = designated illumination area.

The most important factors in the development of solar cells are their efficiency and their production cost. A critical factor affecting the efficiency is the minority carrier lifetime. The minority carrier lifetime is a measure of how much of the injected carriers can contribute to the electric current and it will be defined further in section 2.5. For highly efficient solar cells, the largest cost lies in the refinement of the silicon used in the production. In the refinement process, the silicon has to be melted and re-crystallised for the silicon to become single-crystalline. This processing step requires significant amount of energy.

2.3 Alternative materials and methods

There are various other materials and methods that have been used for research and development of solar cells. These materials can roughly be divided into organic and inorganic materials. The organic materials include polymers which have the potential of being produced inexpensively (Shaheen et al., 2005). The inorganic materials include silicon (single-crystalline, multi-crystalline, amorphous, micro-crystalline, ribbon), the chalcopyrite compound copper indium gallium diselenide (CIGS), the III–V compound semiconductors and lastly CdTe. In general, the organic materials are less expensive and easier to manufacture than the inorganic materials (Shaheen et al., 2005). However they suffer from lower efficiency and shorter minority carrier lifetimes.

The III–V materials, such as GaAs, InP and GaSb, have the advantage over silicon that they have a direct energy bandgap, high optical absorption coefficients, good minority carrier lifetimes, high mobilities (for crystalline materials) and thus the potential to be made into highly efficient solar cells. The disadvantage of the III–V compounds is that the cost of producing high quality substrates and epitaxial layers is high, which gives silicon a head start. Table 2.2 gives an overview of the

Table 2.2: An overview of the advantages and disadvantages of using silicon for solar cells instead of other materials.

Advantages	Disadvantages
Inexpensive and abundant	Narrower bandgaps than for example GaAs and CdTe
Possible to use inexpensive MG-Si substrates	Lower efficiency due to indirect bandgap
Very well established and high reliability	Relatively low electron mobility compared with semiconductors such as Ge, GaAs, GaSb, InP and InAs
Ease of processing	
Non-toxic	
High quality oxide for isolation layers	

advantages and disadvantages of using silicon over other semiconductors in solar cell applications. Amorphous silicon (a-Si), CdTe and CIGS have bandgaps in the range 1.1 – 1.7 eV, so they are near the optimum bandgap energy for photovoltaic solar energy conversion (1.5 eV) by a single junction cell (Miles et al., 2007).

Multi-crystalline silicon is made by melting silicon and then allowing it to cool down in a rectangular container. An advantage of this method over the standard Czochralski method, commonly used to growth single crystalline silicon ingots, is the higher packing density per wafer area and much lower costs when compared with the traditional circular wafers. Multi-crystalline sheets and ribbons can also be fabricated by pulling the sheets from a silicon melt. An obvious advantage of this method is that the sawing can be avoided altogether. Bell and Kalejs (1998) discuss several techniques for growing silicon sheets as substrates for solar cells. This method provides an efficient use of silicon. An example of new silicon based structures for solar cell applications are low cost mechanically flexible solar cells made from ultra thin single-crystalline silicon (Yoon et al., 2008; Fan and Javey, 2008).

Solar cells made of thin film a-Si are produced with plasma enhanced chemical vapor deposition (PECVD) with silane as the source for silicon. The silicon layers can be deposited onto both glass and flexible substrates as the processing temperature can be relatively low. The amorphous silicon is hydrogenated where the hydrogen passivates the dangling bonds that result from the random arrangement of the silicon atoms (referred to as a-Si:H) in contrast to crystalline silicon (c-Si). Hydrogenated amorphous silicon has a direct optical band-gap of 1.7 eV and an optical absorption coefficient greater than $10^5\,\mathrm{cm}^{-1}$ for photons with energy greater than the bandgap. Therefore the thickness of the film needs only to be a few nanometers in order to absorb most of the incident light. With this method, material usage can be reduced and therefore the cost. However, the efficiency is relatively low, the highest reported only 9.5%.

Single junction Si solar cells can lose up to 56% of the available energy due to the fact that photons with energy less than the bandgap are not absorbed and photons with energy higher than the bandgap contribute to heating of the cell. Multijunction solar cells were created to minimize these effects and increase the efficiency. In 1990 a GaAs/GaSb multijunction cell was created that had an efficiency greater than 30% (Miles et al., 2007). Since then multijunction cells using for example GaInP, GaInAs on a variety of substrates have been shown to have efficiency greater than 39% (Miles et al., 2007). However, these are very expensive to manufacture. Solar cells based on CdTe and CdS have been shown to have efficiencies up to 16.5%. The CdTe layers need only to be a few microns thick, which lowers the material costs. CIGS solar cells have a direct bandgap and a high optical absorption coefficient (Mickelsen et al., 1984) and therefore the layers can be thin in order to absorb the incident light. CIGS solar cells have been fabricated with efficiencies up to 19.5% and module efficiencies up to 13.4%.

2.4 Silicon

Silicon exists in various forms that include single crystalline, poly-crystalline or amorphous. In this work, we use metallurgical-grade silicon (MG-Si) which is relatively impure poly-crystalline silicon which is described further in section 4.1.

2.4.1 Crystallinity and defects

An ideal single crystal has a lattice structure that is continuous and unbroken and a replica of the fundamental lattice structure that represents the particular crystal structure. All unit cells in the crystal structure have the same orientation. Poly-crystalline or multi-crystalline materials are composed of many small crystals called grains. Multi-crystalline silicon is processed silicon where the material consists of crystal grains that are typically several millimeters in size. Metallurgical grade silicon (MG-Si) is multi-crystalline silicon that has not been purified and thus it contains a higher concentration of impurities than all the other types. The grains can be oriented randomly or they can have a preferential direction and the material is said to have a texture. Grain boundaries are the regions between the grains. The boundaries are considered to be interfacial defects as they tend to decrease the electrical and thermal conductivity.

All silicon is impure to a certain degree and contains a relatively large amount of defects. A defect can be either an imperfection in the crystal lattice or an impurity that is either added intentionally or was previously in the crystal. Defects can act as recombination centers and trap charge carriers. Point defects can be vacancies or interstitials. An impurity point defect can be substitutional or interstitial. Often defects are created during growth, which depends on the growth conditions and the nucleation site used.

There are three main grades of purity for silicon. The purest is electronic grade

silicon (EGS) which is 9 – 11N. Then it is solar grade silicon which is 5 – 7N and finally MG-Si which is around 2N. Along a grain boundary, the atoms are bonded less regularly than within the grains and therefore carriers can get trapped there. Grain boundary atoms also tend to be more chemically active than those within the grains and thus can act as nucleation sites during growth.

2.4.2 Manufacturing methods

The production cost of a solar cell is composed of the manufacturing cost, cost of materials and the type of system. Two important factors regarding solar cells today are cost and efficiency, but ultimately the important parameter is the cost per watt of electrical energy produced. Silicon is widely available in nature which makes the fabrication of raw silicon relatively inexpensive. The purification of the silicon for use in solar cells, is however the most expensive part of the process.

The production process of silicon starts with a reaction of high-purity quartz with wood charcoal or coal, in an electric arc furnace. In this carbothermic process, the temperatures exceed 1900°C and the carbon reduces the silica to silicon according to

$$\mathrm{SiO_2 + C \rightarrow Si + CO_2}$$

or

$$\mathrm{SiO_2 + 2C \rightarrow Si + 2CO}$$

At the bottom of the furnace, the liquid silicon is cooled down, and the product is multi-crystalline metallurgical-grade silicon referred to as MG-Si. Typical MG-Si chunks are shown in figure 2.5. It contains a relatively large amount of impurities (1–2 %wt) which would normally affect the electrical performance of devices. The main impurities in MG-Si are aluminum (500 ppm), boron (30 ppm), phosphorous

(39 ppm), calcium (92 ppm), iron (230 ppm) and oxygen (4000 ppm) (Wan et al., 2006; Morvan and Amouroux, 1981). The next step in the process of purifying the silicon is mixing HCl with pulverized MG-Si to form trichlorosilane ($SiHCl_3$). Most of the impurities are removed by distillation of the trichlorosilane liquid. A hydrogen reduction reaction is then applied to obtain solid silicon. The resulting material is 99.999% (5N) pure polycrystalline silicon and has impurity concentrations of the order of few parts per billion. To obtain single crystal silicon of still higher purity, the Czochralski technique is generally used (Pearce, 1988). It is based on melting the electronic grade silicon and re-crystallizing it by pulling a seed crystal from the melt. Often an external magnetic field is used to control the amount of unwanted impurities (Sze, 2002). The float-zone process can be used instead of the Czochralski technique to grow single crystal ingots and the resulting ingots have lower impurity concentration than those grown with the Czochralski technique and longer carrier lifetimes, if multiple passes are performed along the rod (Sze, 2002). In that case a high purity poly-crystalline silicon rod is rotated in a chamber in an argon atmosphere. A seed crystal placed at the bottom of the rod determines the crystal orientation. A radio-frequency induction heater is used to melt a portion (zone) of the rod, and moves upwards. A single crystal grows as the melt solidifies below. This method allows for more purification than the Czochralski process by doing multiple passes of the heater along the ingot. The latter method is referred to as zone-refining. Braga et al. (2008) gives an overview of the current status of production of solar-grade poly-crystalline silicon. By using wafers made from MG-Si instead of wafers made from solar grade silicon as a substrate for a solar cell, the cost can be reduced dramatically. Upgraded metallurgical grade silicon (UMG-Si) is produced by leaching and purifying MG-Si followed by a casting process. The result is a multi-crystalline silicon, about three orders of mag-

nitude less pure than SGS, or 2 – 4N (Einhaus et al., 2000). The leaching process is based on detecting impurities such as Fe, Al, Ti and O and vary their proportions (Hötzel et al., 2000). The presence of transition metals in silicon is known to decrease the minority carrier diffusion length (Davis et al., 1980). Buonassisi et al. (2005) show that the predominant metal nano defect in multi-crystalline silicon is $FeSi_2$ ($\sim$ 20 – 30 nm in diameter) and they are found in both grain boundaries as well as structural defects in grains. Also Fe_2O_3 clusters, several micrometers in size are observed. They suggest that if the majority of the transition metals can be contained in micrometer-sized inclusions, and the average distance between the inclusions is kept large enough they cannot interact and therefore they do not have direct impact on the minority carrier diffusion length.

Prior to 2002 the wafer thickness for solar cell production had decreased from

Figure 2.5: The MG-Si rocks that were used as the starting materials for the substrates. In a traditional process, they are melted and re-crystallized to produce solar-grade silicon.

500 μm to 300 μm, which is still considered relatively thick. Shortages of silicon affecting the industry in 2004 pushed wafer thicknesses further down and as of 2007 the wafer thickness for some manufacturers was 200 μm or thinner (Swanson, 2007). Existing photovoltaic technologies use relatively thick silicon wafers of high purity single-crystalline silicon. The use of poly-crystalline silicon is increasing and it is currently the dominating material for solar cells (Braga et al., 2008; Miles et al., 2007). For that reason it is being investigated how it is possible to decrease the amount of silicon used instead of focusing on improving the performance. By using thinner wafers, materials costs can be reduced because most of the optical absorption takes place in the upper 30 μm of the grown film (Poortmans and Arkhipov, 2007).

2.5 Electrical characteristics

Here, we describe the main principles behind the operation of the solar cell and p-n junctions in semiconductors. First we discuss charge carriers in semiconductors, then charge transport in semiconductors, and finally p-n junctions and solar cells.

2.5.1 Semiconductors and p-n junctions

There are two types of charge carriers in semiconductors: electrons and holes. The electron carries a negative charge and the hole (which is always located at the site of a missing electron), behaves as if it is carrying a positive charge. Electrons move in opposite directions of holes in the presence of an electric field. A pure semiconductor crystal, such as silicon does not have available free electrons for current conduction at zero temperature, that is, the conduction band is empty and the valence band is full. At higher temperatures the thermal energy of the crystal

is sufficient to break electron bonds for some conduction to take place. Silicon is of valence 4 and if atoms of valence 5 are added to the silicon crystal, it is easy to ionize and it creates free electrons. Such atoms are referred to as donors. Similarly, adding atoms of valence 3 to silicon crystals leads to holes in the valence band. Such atoms are referred to as acceptors. These extra electrons are added to the conduction band and are available for electron conduction. As said before, a hole is a vacant site of an electron in the valence band and when electrons and holes have a close encounter they recombine. An electron-hole pair can be created by removing a bound electron from a neutral atom. In a pure semiconductor, the minimum energy required to create an electron-hole pair is equal to the bandgap energy of the semiconductor. Electron-hole pairs are created by thermal vibrations of the crystal at any non-zero temperature and also by absorption of photons that have energy above the bandgap energy. The latter is the process that is behind the operation of the solar cell. The production rate of electron-hole pairs is proportional to the intensity of the incident light.

Charge carriers can move under two influences: carrier drift and carrier diffusion. A potential difference between two points in a semiconductor creates an electric field between the two points. The charged carriers, either the electrons or the holes, will be accelerated due to the field until they hit a scattering center. The carriers will have average drift velocity along the lines of the electric field. How easily the charges can move through the crystal structure in the presence of an electric field is described by a parameter referred to as mobility. Scattering of electrons can affect the transport of charge carriers and therefore the mobility. Scattering lowers the energy and momentum of the carriers. Two scattering mechanisms worth mentioning are impurity scattering and lattice scattering. Impurity scattering is due to both intentional dopant impurities and unwanted impurities.

Lattice scattering is due to vibrations and imperfections in the crystal lattice. The trapping of charge carriers depends on the energy of the charge carrier at the trapping/impurity atom. The carrier is trapped if its energy is lower at the trapping site than anywhere else. The electric drift current density in an semiconductor is

$$J_{\text{drift}} = (qn\mu_n + qp\mu_p)\,\mathcal{E} = \sigma\mathcal{E} \tag{2.1}$$

where σ is defined as the conductivity, μ_n and μ_p are the electron and hole mobilities respectively, n and p are the carrier concentrations of electrons and holes respectively, q is the electron charge and $\mathcal{E}$ is the electric field strength. Carrier diffusion is due to a carrier concentration gradient in the semiconducting material. The diffusion current density is

$$J_{\text{diff}} = qD_n\frac{dn}{dx} - qD_p\frac{dp}{dx} \tag{2.2}$$

where D_n and D_p are the electron and hole diffusion coefficients respectively. The total current density due to drift and diffusion is

$$\begin{aligned} J_{\text{total}} &= J_{\text{drift}} + J_{\text{diff}} && (2.3)\\ &= (qn\mu_n + qp\mu_p)\,\mathcal{E} + qD_n\frac{dn}{dx} - qD_p\frac{dp}{dx} && (2.4)\\ &= \left(qn\mu_n\mathcal{E} + qD_n\frac{dn}{dx}\right) + \left(qp\mu_p\mathcal{E} - qD_p\frac{dp}{dx}\right). && (2.5) \end{aligned}$$

In solar cells, excess carriers are introduced by optical absorption of the semiconducting material, a process often called carrier injection. In this situation, the system is not in thermal equilibrium, that is, $pn > n_i^2$, where n_i is the intrinsic carrier concentration. For equilibrium to be regained, minority and majority carriers recombine. The dominating recombination process for silicon is an indirect

process because of the indirect band-gap of silicon. When a semiconductor material is illuminated, electron-hole pairs are generated with a rate G_{L}. At equilibrium, the generation rate is equal to the recombination rate, $G_{\mathrm{L}} = R = G_{\mathrm{th}}$. The net recombination rate is $U = R - G_{\mathrm{th}}$ and is equal to zero at thermal equilibrium. For holes in an n-type semiconductor, the net recombination rate is proportional to the excess minority carrier concentration, or

$$U = \frac{p_n - p_{n0}}{\tau_p} \tag{2.6}$$

where τ_p is the minority carrier lifetime and is a measure of how fast majority and minority carriers recombine, p_{n} is the minority carrier concentration and p_{n0} is the minority carrier concentration at thermal equilibrium. The minority carrier lifetime is an important parameter for solar cells as it is used as a measure of the quality of the cell. The minority carrier lifetime can be estimated by illuminating a semiconducting sample and measure the open-circuit voltage decay. If a short light pulse is used to illuminate an n-type semiconductor, then the minority carrier concentration after the light pulse is turned off is

$$p_n(t) = p_{n0} + \tau_p G_{\mathrm{L}} \exp\left(-t/\tau_p\right). \tag{2.7}$$

Figure 2.6 shows a schematic of a p-n junction along with a graph that shows the minority carrier concentration in the n- and p-side of the junction respectively, with and without light injection. For solar cells, it is important that the recombination does not occur before the carriers reach the p-n junction. The method used to measure the minority carrier lifetime will be discussed in chapter 3.4. The relation between diffusion length L_{p} of holes in the n-type semiconductor and the minority

carrier lifetime is given by

$$L_{\mathrm{p}} = \sqrt{D_{\mathrm{p}} \tau_{\mathrm{p}}} \tag{2.8}$$

where D_{p} is the diffusion coefficient of holes. The short-circuit current in solar cells can decrease due to the recombination of charge carriers at a boundary (Zook, 1980). As the grain size decreases, electrical parameters such as minority carrier lifetime decrease (Yamazaki et al., 2006).

p-n junction

A junction of opposite charge carrier types can be created in semiconductors. When the junction is formed, the electrons diffuse to the p-side and holes diffuse to the n-side. This is due to carrier concentration gradients near the junction. Uncompensated donor and acceptor sites are left behind in the n- and p-side, respectively. Donors on the n-side are ionized and thus positively charged. Similarly, on the p-side, acceptors are ionized and thus negatively charged. This creates an electric field in that region which is called the space-charge region or depletion region. The potential difference between the n- and p-side is called the built-in potential. It depends upon the doping concentrations in the p-type and n-type semiconductor materials. The width of the depletion region also depends on the doping concentration.

When the p-side of a p-n junction is at a higher potential than the n-side, that is the junction is forward biased, minority carriers are injected into each side. The potential across the depletion region is lowered and the current across the junction consists mainly of diffusion. Under reverse bias, the built-in voltage is raised and the resulting drift current is very small and is referred to as reverse current. Figure 2.7 visualizes an energy band diagram for a p-n junction in thermal equilibrium. The potential barrier between the n- and p-side is qV_{bi}. The ideal diode equation

gives the current through the p-n junction for forward and reverse bias

$$I = I_{\mathrm{s}} \left(\exp \left(qV/nkT \right) - 1 \right) \tag{2.9}$$

where n is the ideality factor and I_{s} is the reverse saturation current, given by

$$I_{\mathrm{s}} = qA \left(\frac{D_{\mathrm{p}} p_{\mathrm{n}}}{L_{\mathrm{p}}} + \frac{D_{\mathrm{n}} n_{\mathrm{p}}}{L_{\mathrm{n}}} \right). \tag{2.10}$$

Solar cells and photodiodes

When a photon hits a semiconductor surface, an electron in the valence band can be excited into the conduction band. This process is called photon absorption and is strongest when the electron can go directly to the conduction band. For semiconducting materials with an indirect bandgap, lattice vibration are required to assist in the process. The absorption coefficient α describes the ability of the

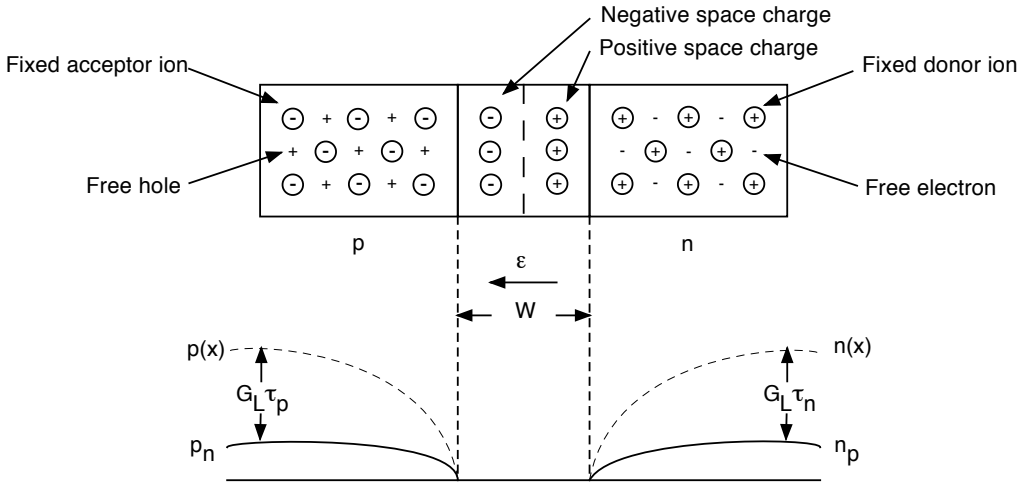


Figure 2.6: Minority carrier concentration in an p-n junction with (dashed line) and without (solid line) light injection.

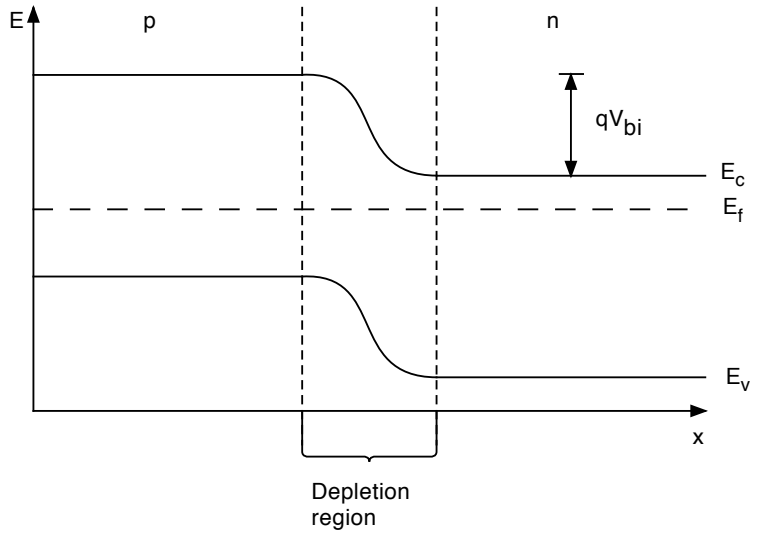


Figure 2.7: An energy band diagram of an p-n junction in thermal equilibrium.

material to absorb photons. Below the bandgap energy E_g the semiconductor is transparent and the absorption coefficient is zero. Similarly above a specific cutoff wavelength λ_c the absorption coefficient is zero. It is given by

$$\lambda_c = \frac{1.24}{E_g} \tag{2.11}$$

where E_g is in eV and λ_c is in μm. The band gap energy of silicon is 1.12 eV at room temperature. Therefore photons with energy less than the bandgap energy of silicon are not absorbed. Photon energy higher than 1.12 eV corresponds to wavelengths less than 1.11 μm and therefore ranges from the near-infrared to the ultra-violet region. When photons of energy larger than the band gap energy of the semiconductor, hit the surface of a semiconductor, electron-hole pairs are generated. Photons of energy that is much larger than the bandgap energy of the semiconductor lose part of their energy as heat. For absorbed photons in the

semiconductor, the carrier generation rate is

$$G_{\mathrm{L}} = \frac{\alpha P_{\mathrm{op}}}{\hbar\omega} = \alpha J_{\mathrm{ph}}(x) \tag{2.12}$$

where $J_{\mathrm{ph}}(x)$ is the photon flux, P_{op} is optical power per unit area, α is the absorption coefficient and $\hbar\omega$ is the photon energy. This is referred to as photoconductivity. The responsivity of the semiconductor to incoming photons is given by (Singh, 2001)

$$R_{\mathrm{ph}} = \frac{J_{\mathrm{L}}}{P_{\mathrm{op}}} \tag{2.13}$$

where J_{L} is the resulting photocurrent density. The absorption coefficient α for direct bandgap materials is typically a factor of 100 higher than for indirect bandgap materials (Singh, 2001).

A p-n junction solar cell is in principle composed of a p-n junction near the surface of the diode (shallow junction) and ohmic contacts to the front and back of the diode. A schematic of a solar cell is shown in figure 2.8. The ohmic contacts on the front surface are called bus bars and are used to provide ohmic contacts with minimum series resistance and without shadowing the incoming radiation. The junction must be near the surface of the grown film for most of the minority carriers to be able to reach the junction before they recombine with the majority carriers. If a minority carrier reaches the junction, it is swept across the junction by the electric field resulting in an electric current. The diffusion length of the minority carriers is a measure of how far they diffuse before recombining. Therefore it is required that the diffusion length is larger than the distance from where they are created, to the junction. The power solar cells can convert is proportional to the power of the incident light and the area of the cell. Photodiodes as well as solar cells are based on p-n junctions that collect the carriers that are injected into one side. The

minority carriers diffuse to the space charge region of the junction and are swept across this region by the built-in electric field. The difference between solar cells and photodiodes is that the photodiode requires reverse bias for its operation. Thus photodiodes operate in the first quadrant of the $I-V$ characteristics while solar cells operate in the third quadrant. Figure 2.9a shows a typical $I-V$ characteristic for a solar cell. Figure 2.9b shows the $I-V$ characteristic in the fourth quadrant after inversion about the voltage axis.

An equivalent circuit of a solar cell and a load connected to it is seen in figure 2.10. The current through the solar cell is given by (Schwartz, 1993)

$$I = I_{\mathrm{L}} - I_{\mathrm{s}}\left(\exp\left(\frac{q(V+IR_{\mathrm{s}})}{nkT}\right)-1\right) - \frac{V+IR_{\mathrm{s}}}{R_{\mathrm{shunt}}} \tag{2.14}$$

where I_{s} is the reverse saturation current, V is the voltage across the cell, n is the ideality factor and I_{L} is the photon induced current. The ideality factor is equal to 1 for an ideal diode and increases as the quality of the diode decreases.

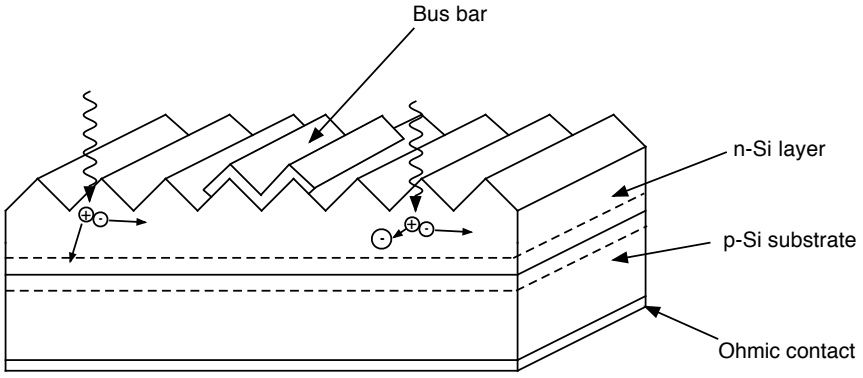


Figure 2.8: A schematic of a p-n junction solar cell along with the front and back ohmic contacts. On the left an incoming photon generates an electron-hole pair, the hole diffuses across the junction and contributes to the current. On the right, the hole from the generated electron-hole pair is trapped by an impurity and does not contribute to the current.

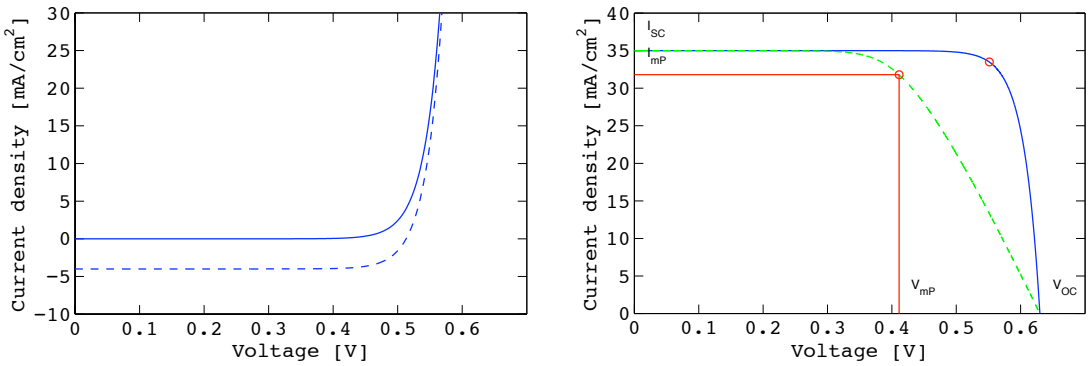


Figure 2.9: Figure (a) shows the $I-V$ characteristics of a solar cell with (dashed line) and without illumination (solid line). Figure (b) shows quadrant IV and the solid blue line shows the $I-V$ characteristics for an ideal solar cell. The dashed green line shows the $I-V$ characteristic for a solar cell with $R_{\mathrm{S}} = 5\,\Omega$ and $R_{\mathrm{shunt}} = 1\,\mathrm{M}\Omega$. The square shows the area where maximum power can be drawn from the device.

R_{s} represents the series resistance of the diode and R_{shunt} represents the diodes internal characteristic. For an ideal diode, $R_{\mathrm{s}} = 0$ and $R_{\mathrm{shunt}} = \infty$. The series resistance results from ohmic losses in the front surface. A series resistance of $5\,\Omega$ can reduce the available power by 30% compared to the ideal case (Sze, 2002). The series resistance depends on the depth of the junction, the impurity concentration in the p- and n-regions and the arrangement of the ohmic contacts. An increase in R_{s} causes a reduction in V and I_{sc}. Low values in R_{shunt} can be caused by an increased conductance through the diode. This has the effect of decreasing the current and reducing the open-circuit voltage. The ideality factor of the solar cell can be estimated by calculating the slope m of the positive part of $\ln I$ as a function of applied voltage. Then the ideality factor is calculated as

$$n = \frac{q}{kTm}. \tag{2.15}$$

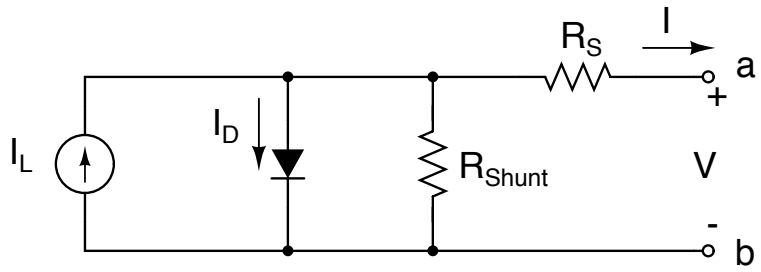


Figure 2.10: Equivalent circuit of a solar cell. I_{L} is the photon induced current, I_{D} is the ideal diode current, R_{S} is the series resistance and R_{shunt} is the shunt resistance of the diode.

For an ideal diode, the open circuit voltage ($I = 0$) is

$$V_{\mathrm{OC}} = \frac{kT}{q} \ln\left(\frac{I_{\mathrm{L}}}{I_{\mathrm{s}}} + 1\right) \tag{2.16}$$

and the power that the solar cell absorbs and converts is

$$P = IV = I_{\mathrm{L}}V - I_{\mathrm{s}}V\left(\exp\left(\frac{qV}{nkT}\right) - 1\right). \tag{2.17}$$

The maximum power P_{m} is absorbed when $dP/dV = 0$, or at $P_{\mathrm{m}} = I_{\mathrm{m}}V_{\mathrm{m}}$. The power conversion efficiency is given by

$$\eta = \frac{I_{\mathrm{m}}V_{\mathrm{m}}}{P_{\mathrm{in}}} \tag{2.18}$$

or

$$\eta = \frac{\mathrm{FF} \cdot I_{\mathrm{SC}}V_{\mathrm{OC}}}{P_{\mathrm{in}}} \tag{2.19}$$

where P_{in} is the solar power incident on the cell and FF is the so called fill factor defined as

$$\mathrm{FF} = \frac{I_{\mathrm{m}}V_{\mathrm{m}}}{I_{\mathrm{SC}}V_{\mathrm{OC}}}. \tag{2.20}$$

For the efficiency to be maximized, the product of FF and $I_{\mathrm{L}}V_{\mathrm{OC}}$ has to be maximized (Schwartz, 1993). For most solar cells, the fill factor is FF ≈ 0.7. Hötzel et al. (2000) discusses how the fill factor can be optimized. The thermodynamic efficiency limit describes how photons with energy greater than the band-gap of the silicon can be converted to electricity, while photons with energy well above the band-gap are mostly converted to heat. Only a fraction of the photons with energy above the band-gap are converted to electricity, and the rest is converted to kinetic energy. This problem can be partially solved by utilizing multiple band-gap absorber materials which increases this efficiency (Schwartz, 1993). Quantum efficiency is referring to the part of the photons that are converted to electric current. Internal quantum efficiency is the fraction of absorbed photons that are converted to electric current, while external quantum efficiency is the fraction of incident photons that are converted to electric current.

2.6 Creation of an active layer

From the 1950s and onwards, p-n junctions are typically fabricated by diffusion of impurities or dopants into a bulk material which can be silicon. This can be done in various ways, for example by placing a silicon wafer inside a chamber along with a gas that contains an impurity that would act as an acceptor or a donor and thus give the appropriate doping. By annealing for specific amount of time, the dopant diffuses a certain distance into the substrate. One disadvantage of this method is that the p-n junction will be graded instead of abrupt. In addition, if the substrate is poly-crystalline, the dopants can diffuse faster along the grain boundaries, creating channels of dopants. Consequently the depth of the junction and the thickness of the solar cell will be relatively large which will lower the efficiency due to recombination of electrons and holes.

Another method is ion implantation, in which the dopant ions are accelerated into the grown silicon film. A disadvantage of this method is that the surface gets damaged during the ion bombardment. This can be partially fixed by annealing the substrate which in turn drives the junction deeper into the substrate, which is an disadvantage for solar cells because the junction has to be close to the surface in order for the charge carriers to reach the junction before they recombine.

A p-n junction can also be fabricated by growing a doped thin film semiconductor on top of a substrate of the opposite doping type. This is the method discussed here.

Chapter 3

Experimental methods and apparatus

Here, the instruments and equipment used as well as the methods applied for the thin film growth and thin film characterization are described. First, the liquid phase epitaxy (LPE) technique is discussed in general and then its applications to silicon thin film growth. Subsequently, hydrogenation of the grown films is discussed. An overview of the electrical characterization is given, including the measurements of minority carrier lifetime and the Hall and conductivity measurements that give the carrier concentration and mobility, respectively. A scanning electron microscope (SEM) and an atomic force microscope (AFM) are used to assess the film morphology. Finally the crystallinity of the films and substrates are characterized using X-ray diffraction (XRD).

3.1 Liquid phase epitaxy

Liquid-phase epitaxy (LPE) is a method to grow crystalline layers from a melt on solid substrates. The melt is usually a metal which can dissolve the needed amount of the growth material. Common solvents used for silicon growth include tin (Sn), gallium (Ga) and indium (In). A more thorough discussion of solvents in silicon LPE will be in section 3.1.3. In principle, LPE can be applied to any chemical system where a sufficient amount of solute material can be precipitated from the solvent during cooling. In this way a film can be formed on a substrate.

Many variations in LPE growth exists (Astles, 1990; Scheel, 2007). These include the vertical dipping method, where the substrate is dipped into the metal solution and the slider-boat method, where the substrate is dragged through crucibles which contain appropriate liquid metal solutions. In the slider-boat method, the substrate is held in place with a special kind of a fork. Crucibles are lined up and the substrate can be dragged under the crucibles for the substrate to come into contact with the materials contained in the crucibles. The crucibles and the fork are usually made of graphite because it can withstand high temperatures without decomposing and contaminating the growth. This method is suitable for laboratory use but not for large-scale production. The dipping method is more suitable for large-scale production because the crucibles and substrates can be very large and thus larger batches can be produced.

LPE is not suitable for growing layers in the nanometer thickness scale due to the high surface tension of metallic solutions of semiconductors (Scheel, 2007). Therefore it cannot be used for fabrication of transistors or other similar delicate structures. Furthermore, LPE is not suitable for applications that require large-area uniformity, critical layer thickness and composition control. Other techniques such as chemical vapor deposition (CVD), molecular beam epitaxy (MBE) and

metal-organic vapor phase deposition (MOVPE) are often chosen instead and are discussed in section 3.1.1. The LPE technique offers many advantages over other deposition methods. It is simple and the operating and equipment costs are relatively low. The films are of good quality with low contamination levels even when grown at relatively low temperatures. Low density of structural defects and low recombination activity at grain boundaries can be obtained if the growth conditions are suitable. Furthermore, LPE offers high deposition efficiency. The technique was originally invented to overcome limitations of substrate quality as well as the limitations of the CVD technique (Mauk, 2007). There are no toxic precursors or byproducts involved with the LPE process as for instance in MOVPE and CVD, and the quality of the grown layers with respect to minority carrier lifetimes and recombination lifetimes, is high, which is important for solar cell applications (Mauk, 2007). LPE can be a suitable method for thin film growth on low-cost substrates. The substrate can be in-situ etched by partial dissolution of the substrate in the metal solvent, often referred to as melt-back. If the slider-boat technique is used, this can be implemented by dragging the substrate under a crucible containing a metal solvent partly saturated with the growth material. This can improve the wetting of the substrate before growth and reduce the occurrences of so called growth pyramids. Growth pyramids are due to twinning which is often initiated at the substrate surface (Ghandhi, 1983). Pyramidal textures can though be of use in light entrapment as demonstrated by Konuma et al. (1994) which had success with growing pyramidal and roof shaped textures on silicon for these purposes.

LPE has mostly been used for growing GaAs , GaP and AlGaAs thin films, and also silicon on a variety of substrates (Mauk, 2007). For solar cell applications the substrate can be for example single-crystalline (Zheng et al., 1996; Arch et al., 1993; Majumdar et al., 2003), poly-crystalline (Steiner and Wagner, 1995), upgraded

metallurgical grade silicon (Ciszek et al., 1993; Hötzel et al., 2000; Peter et al., 2002; Kopecek et al., 2001; Müller et al., 2003) and with a porous sacrificial silicon layer (Fave et al., 2008). Abrupt p-n junctions can be created when growing films with the LPE method. A wide range of dopants are available. The growth temperature can be well below the melting point of the growth material, which is of great importance since high temperatures can cause decomposition of the substrate. A disadvantage of using LPE for growing silicon thin films is that the solubility of silicon in many metallic melts is low and there can be high content of the solvent incorporated into the grown film. To reduce material costs, the solvents can in principle be reused.

One restriction to the use of LPE is the limited amount of lattice mismatch between the substrate and the grown layer which can be tolerated. The lattice mismatch is defined by

$$\mathcal{E} = 2\frac{a_\mathrm{l} - a_\mathrm{s}}{a_\mathrm{l} + a_\mathrm{s}} \tag{3.1}$$

where a_l and a_s are the lattice parameters of the layer and substrate respectively. If $\mathcal{E} > 10^{-3}$ then an increasing tendency towards the generation of misfit dislocations and an increasing difficulty in nucleating the epitaxial layer growth is expected (Astles, 1990). The effects of thermal mismatches are increased when the silicon layer is grown on a foreign substrate (Abdou et al., 2005). Such lattice mismatch is most easily avoided by growing film with similar or same lattice parameter as the substrate. The MG-Si substrate that is being used in our case can be considered a foreign substrate to a certain degree.

A summary of the main advantages and disadvantages of LPE is given in table 3.1.

Table 3.1: An overview of the advantages and disadvantages of liquid-phase epitaxy for the growth of silicon thin films.

Advantages	Disadvantages
High quality of grown films	Solubility of silicon in many metallic melts is low
Relatively low growth temperatures compared to other methods	High content of solvent can be incorporated into the grown film
Abrupt junctions	Hard to control layer thickness and uniformity
High growth rates compared with other thin-film techniques	Not suitable for growing layers in nanometer scale
High deposition efficiency, and low equipment and operating costs	Only a small lattice mismatch between substrate and film is tolerated
No toxic precursors	Difficult to monitor the growth process directly
In-situ etching of silicon and in-situ doping	Non-uniform thickness
Wide range of dopants	
Reusable solvents	

3.1.1 Alternatives to LPE

When selecting a method for epitaxial growth of specific materials and for particular applications, some practical considerations must be followed. They include capital investment, operating costs, safety, reproducibility, required skill and controllability with respect to thickness and doping (Astles, 1990). A number of methods are currently being used for both research and production of solar cells. These include MBE, MOVPE and CVD. In the recent years, the requirement of large area uniformity, critical layer thickness and composition control, smooth surfaces and abrupt interfaces, has pushed the LPE technique off the market replacing it by MBE and MOVPE which can fulfill the requirements. There is though a constant development of the LPE technique and control over the grown layer thickness is improving.

In LPE the composition of the layer is determined by phase equilibria and thus exhibits a low thermodynamic driving force. Consequently better control of nucleation is obtained which is necessary for selective modes of growth, it also lowers the possibility of nucleation on non-equilibrium defects such as stacking faults and dislocations.

MBE is a method for epitaxial growth based on reactions of thermal beams of atoms or molecules with a crystalline substrate under a high vacuum. MBE is precise in both chemical compositions and doping profiles. Multilayer structures with thickness on the order of atomic layers can be grown. However, the deposition rate is very low.

CVD, often referred to as vapor phase epitaxy (VPE), is a method in which epitaxial layers are grown by reactions between gaseous compounds. Metal-organic vapor phase epitaxy (MOVPE) varies from the traditional CVD as it is based on surface reactions of metal organic compounds and metal hydrides. MOVPE has mostly been used for heteroepitaxial growth of III–V and II–VI compounds. CVD is a costly and complex method for deposition of silicon (McCann et al., 2001). CVD is scalable and generally allows fabrication of high quality layers. However, at low temperature ($< 600°C$) the deposition rate is low.

MBE and CVD exhibit high thermodynamic forces which as useful for heteroepitaxial growth where there is strain or lattice mismatch that inhibits nucleation of the epitaxial layer. In particular the cost of precursor and dilutant gases is substantial. Most deep level impurities have low segregation coefficients. As a result, epitaxial layers grown with LPE have been shown to have lower deep level incorporation than CVD for example (Ghandhi, 1983). MOVPE offers better control over the grown layer thickness, doping concentration, abruptness of grown interfaces and alloy composition. MBE and MOVPE offer higher supersaturations than possible

in LPE. Higher supersaturation makes it possible to grow single-crystalline films on substrates with high lattice mismatches ($\mathcal{E} < 10^{-1}$) or with different crystal structures (Astles, 1990). Growth rate by LPE can be 10 – 100 times faster than by MBE or CVD and the whole process can be more flexible. Generally, CVD has more experimental parameters than LPE, but a broad operating range. Thus, the LPE method is more susceptible to process fluctuations and the effects of uncontrolled parameters. Both can lead to failed growth or poor material quality. LPE appears to be more sensitive to the crystallographic orientation of the substrate than other epitaxy techniques. When the controllable parameters for LPE growth are within its optimum range, the material quality of the grown layers can be superior to that produced by other epitaxy techniques. Although LPE has not been considered suitable for large scale production, recent modifications have changed the situation (Müller et al., 2003; Weber et al., 2003).

3.1.2 Doping and precipitation from the liquid phase

Almost any solids, liquids or gases that come into contact with the substrate at the growth temperature will be incorporated into the grown film to a certain degree. This emphasizes the fact that the choice of solvent and other ingredients that are used is very important. In some cases, the solvent itself acts as a dopant in the grown film. Types of solvents for silicon LPE will be discussed further in section 3.1.3. A segregation coefficient k_i is a measure of how much of the impurities are incorporated into the solid from the melt. As the starting materials for LPE growth are normally of high purity, the easiest way for impurities to enter the system is through partial substrate dissolution, or melt-back. This improves the wetting of the substrate and helps by removing the native oxide of the substrate. The segregation coefficient of impurities from metal solvents to solid silicon in the

temperature range $800 - 1000°C$ is given by

$$k_{\mathrm{i}} = \frac{C_{\mathrm{i}}^{\mathrm{S}}}{C_{\mathrm{i}}^{\mathrm{L}}} = k_{\mathrm{i},0} \cdot \exp\left(-\frac{b_i}{T}\right) \tag{3.2}$$

where $C_{\mathrm{i}}^{\mathrm{S}}$ is the impurity concentration in the solid silicon, $C_{\mathrm{i}}^{\mathrm{L}}$ is the impurity concentration in the liquid, T is the temperature of the liquid and $k_{\mathrm{i},0}$ and b_i are constants that are specific to each impurity. It depends on the solvent used whether melt-back is necessary, but Gee and Ciszek (1996) report on using a Cu/Al solvent that is able to wet the substrate without melt-back. In the case of using a silicon substrate, the substrate is often etched in a diluted hydrofluoric acid before growth to ensure an oxide free surface. For trivalent solvents such as gallium and indium, their segregation coefficient is relatively high in silicon and therefore they will act as p-type dopants. Tin and lead are iso-electronic with silicon and therefore will not provide charge carriers in the crystal.

An equilibrium binary phase diagram describes the relationship between the compositions of the components and the temperature of the system while the pressure is a constant. In LPE, phase diagrams are useful in determining the solubility of a solute in a specific solvent over a specific temperature range. Additionally they give indication of the behavior of the system with temperature. The Si-Ga phase diagram is shown in figure 3.1. Above the liquidus line, only liquid phase (L) exists and below the solidus line, only a solid phase (α) exists. Between the liquidus and solidus lines is a region in which both liquid and solid phases (L + α) can exist. The solidus line in the phase diagram gives information about the degree of incorporation of the component into the solid (Mauk, 2007). The slope of the liquidus line gives the temperature range for growth to occur. Additionally it gives information on how much of the growth material can be precipitated from the solvent. Typically, the solubility of semiconductors such as silicon in metals

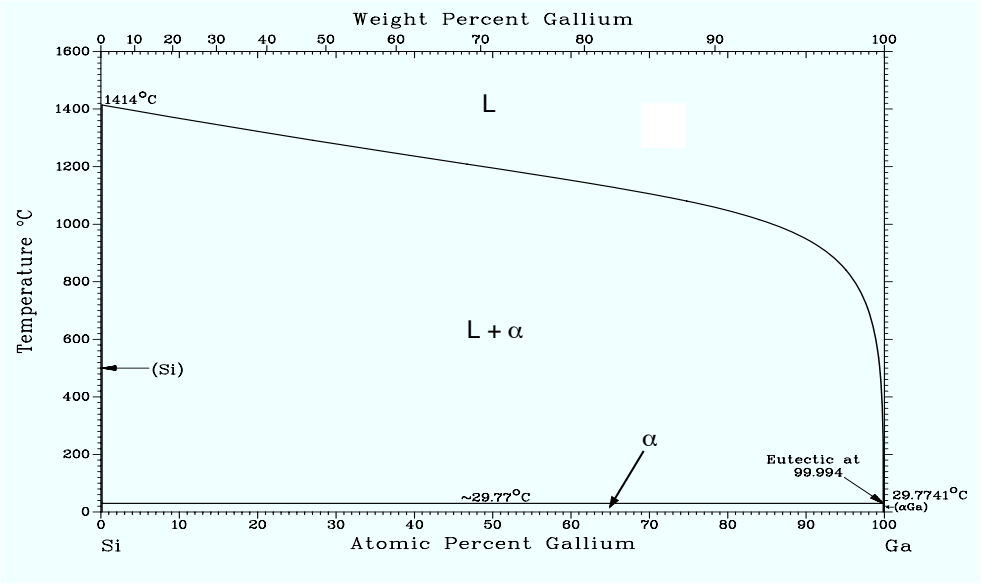


Figure 3.1: The Si-Ga phase diagram which shows the relationship between component concentration and temperature at a constant pressure (ASM, 2008). Above the liquidus line is a liquid phase (L), between the liquidus and solidus lines is a combination of a liquid phase and a solid phase (L+α), and under the solidus line is only a solid phase (α).

increases with temperature.

The solvent is saturated with the solute at the liquidus temperature T_{L}. The driving force of the growth is the supersaturation of the solvent by the solute. The supersaturation can be obtained in different ways. Ramp cooling is based on saturating the solvent at the growth temperature $T_{\mathrm{G}} = T_{\mathrm{L}}$ and decreasing the temperature of the system by $\Delta T_{\mathrm{R}} = T_{\mathrm{G}} - T_0$ with a fixed rate R [°C/min]. In this case the substrate is brought into contact with the solution while the solution is being either saturated with sacrificial silicon or silicon that originates in the substrate. This takes place in the time interval between t_1 and t_2 as shown in figure 3.2. This allows for the solvent to become fully saturated with the solute if it was not before. A larger supersaturation is obtained with the supercooling technique. There the supersaturation of the solvent is increased by decreasing the

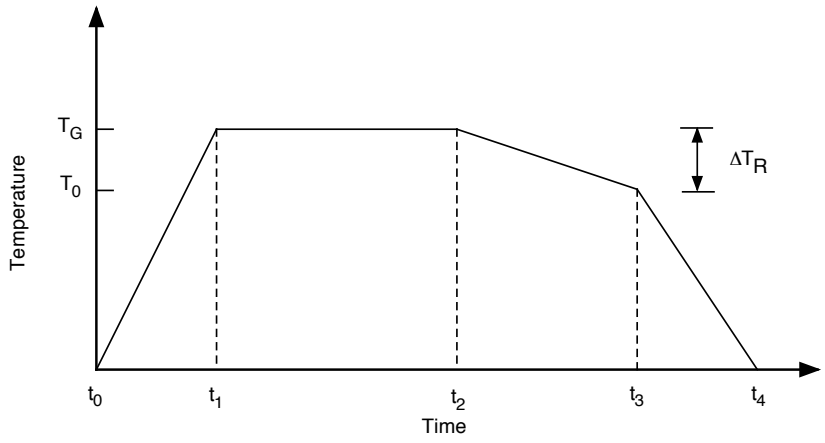


Figure 3.2: Temperature-time profile for ramp-cooled LPE growth. Initially the system is heated up to the growth temperature T_{g}. At t_1 the growth solution is saturated with the solute at the temperature T_{g}. At t_2 the growth starts and ends at $t = t_3$. Between the time t_3 and t_4 the system cools down.

temperature of the system by $\Delta T_{\mathrm{S}} = T_{\mathrm{L}} - T_{\mathrm{G}}$. The substrate is then brought into contact just before the temperature is decreased by $\Delta T_{\mathrm{R}} = T_{\mathrm{G}} - T_0$ with a fixed rate $R\,[^{\circ}\mathrm{C/min}]$. The supersaturation is relieved by precipitation of the solute on a substrate. It is important that there is no excessive silicon present in the saturated melt at the liquidus temperature. The silicon would then act as a nucleation center and compete with the substrate, possibly result in low surface coverage of the grown film. The growth temperature is known to affect the lifetime of minority carriers in LPE grown films. At growth temperatures above 800°C, the minority carrier lifetime decreases drastically as the growth temperature increases (Satoh et al., 2005). It was shown that this reduction in minority carrier lifetime was due to high incorporation of the solvent at higher temperatures. Peter et al. (2002) reports on obtaining smoother layers when the cooling rates are relatively low ($\leq 1^{\circ}\mathrm{C/min}$).

3.1.3 Silicon LPE

Solvents and dopants

When choosing the solvents for epitaxial growth of silicon thin films, there are several criteria that can be used as guidelines (Mauk, 2007).

- The melting point of the solvent has to be relatively low and should be able to dissolve the needed amount of silicon.
- The wetting of the substrate is an important factor in order to obtain a continuous layer.
- There must be low reactivity between the crucible material and the solvent.
- It is preferred that the solvent is non-toxic or at least low in toxicity.
- There must be a simple and versatile way to remove the remains of the solvent from the surface of the grown film.
- The electrical properties of the metal or any metals that are dissolved in the solvent must be known. They can either be iso-electrical or electrically active.

Table 3.2 gives an overview of solvents that can be used for silicon LPE growth. The solvent and any impurities that are dissolved in the melt are incorporated into the grown silicon film, to a certain degree. These impurities are either added to intentionally dope the deposited layer or they can originate in the substrate or from other sources. The melt can also remove impurities that could have resided on the surface of the substrate. Impurities that belong to groups III and V of the periodic table are substitutional diffusers in silicon with the exception of indium (In). The dopants from group III and V are all shallow donors and shallow acceptors in silicon, respectively. Impurities from group I and group VIII take up interstitial sites in

silicon and are usually electrically inactive. An exception is lithium which acts as donor in silicon. Elements such as cobalt, copper, gold, iron, nickel, platinum and silver diffuse by an interstitial-substitutional mechanism in silicon and can end up in both types of sites. All of these impurities are known to reduce minority carrier lifetime in silicon. Silver and gold are deep lying impurities in silicon and gold has been used effectively to reduce minority carrier lifetime in silicon for specialized applications (Ghandhi, 1983).

The solubility of silicon in various metal solvents depends on the nature of the solvent and the temperature. For growing relatively thick silicon films, higher temperatures are required, which on the other hand lowers the minority carrier lifetime (Abdou et al., 2005). Among well known solvents used in silicon LPE are tin (Sn), lead (Pb), gallium (Ga), indium (In), aluminum (Al), bismuth (Bi), antimony (Sb), gold (Au) and copper (Cu). Table 3.2 gives an overview of the previously mentioned solvents, along with some of their properties at 900°C. Impurities such as boron (B) can be difficult to remove from silicon since its segregation coefficient is high compared to other elements as shown in table 3.2.

Table 3.2: Overview of the growth relevant properties of metal solvents for silicon LPE growth for a growth temperature of 900°C (Sze, 2002).

Metal solvent	Melting point [°C]	Segr. coeff.	Solubility [cm^{-3}]	Doping
Aluminum (Al)	660	2×10^{-3}	1×10^{19}	p
Antimony (Sb)	630.8	2.3×10^{-2}	3×10^{19}	n
Bismuth (Bi)	271.4	7×10^{-4} [1]	2×10^{16}	n
Copper (Cu)	1083.2	4×10^{-4}	1×10^{17} [2]	-
Gallium (Ga)	29.8	8×10^{-3}	2×10^{19}	p
Indium (In)	156.2	4×10^{-4}	2×10^{16}	p
Tin (Sn)	231.9	1.6×10^{-2}	4×10^{19}	-

[1]: Morvan and Amouroux (1981)
[2]: Ghandhi (1983)

Growth and substrates

Abdou et al. (2005) studied LPE growth from tin alloys (Sn-Al, Sn-In) at 800°C and reported that adding a trace amount of aluminum to the solvent helps with removing the native oxide of the substrate. For the aluminum not to heavily dope the grown layer, it must be added to a separate melt. Better morphology was obtained with a higher content of Sn in the Sn-In system, but voids on the substrate were existent when using an In rich solvent. Konuma et al. (1995) reports on layer growth on single crystalline silicon substrates with Ga and Ga-In solvents at temperatures below 450°C. Growth from the Ga-In alloy results in a p-type doped layer with carrier concentration that is 50% of the concentration obtained by a Ga solvent alone. Peter et al. (2002) studied the effect of gallium concentration in the In-Ga system on the layer characteristics. A 0.1%wt Ga with In melt resulted in a carrier concentration of around $10^{17}\,\mathrm{cm}^{-3}$ and a smooth layer. The electrical characteristics depended heavily on the growth rate as the mobility and minority carrier lifetime increased as the cooling rate was lowered. Arch et al. (1993) also grew p-type Si layers from In-Ga solvent with carrier concentrations in the range $10^{16} - 5 \times 10^{19}\,\mathrm{cm}^{-3}$. They claim the quality of their films is comparable to that of float zone silicon. Similarly, Zheng et al. (1996) used Ga doped In melt to grow Si film for a highly efficient solar cell. Tin and lead are electrically neutral in silicon and for that reason they are often chosen as solvents. The presence of tin in the melt will though have effect on the electrical parameters as the presence of tin is known to decrease minority carrier lifetime. Weber et al. (2003) report that a significant reduction in minority carrier lifetime is observed in thin films grown from a tin solvent when compared with films grown from an indium solvent. The market supply of solvents is also an important factor when selecting solvents. Weber et al. (2003) mentions that a limited availability of indium causes problems when

upscaling. Ciszek et al. (1993) studied LPE growth of thin film silicon from alloy solvents that included Cu, Al, Al-Cu, Bi, Ga-Cu and Sn solutions at temperatures below 950°C.

Some of the problems that arise when growing Si thin films on multi-crystalline MG-Si substrates include

- rough surfaces from growth rate variation due to variable grain orientation
- impurity contamination from the MG-Si substrate
- solvent sticking to the grain boundaries due to enhanced dissolution at the grain boundaries
- electrical properties due to dopant incorporation and grain size effects

Ciszek et al. (1993) report that in order to obtain smooth layers, the temperature control must be precise and cooling rate must be ≤ 0.2°C/min. Higher cooling rates can lead to solvent entrapments and inclusions in the grown layer. Solution entrapment can in particular be a problem along grain boundaries for low-cost substrates. The low solubility of Si in Bi resulted in lower thickness than required. Layers grown with Sn solvent gave poor results with respect to open-circuit voltage which could have been due to high metal content in the layer. Layers grown from a Cu solvent gave higher J_{sc}, but lower V_{OC} probably due to solution entrapment. Smooth layers were not achieved on MG-Si substrates without melt-back. Copper has previously been known to decrease carrier lifetime in grown layers, but is usable as a solvent (Mauk, 2007). Hötzel et al. (2000) demonstrated successful growth of high quality thin film silicon on UMG-Si substrate using a In-Ga solvent. Melt-back was used and concentration of impurities was not significant. Pure Indium solvent did not give a doping concentration suitable for solar cell applications so gallium was used as a dopant to obtain a carrier concentration of $\mathrm{p} \approx 10^{17}\,\mathrm{cm}^{-3}$.

In this work, growth temperature of 900°C and an alloy of gallium and indium was used as a solvent. These solvents were chosen mainly due to its low melting point and the relatively high solubility of silicon. As seen in table 3.2, gallium and indium are acceptors in silicon. The substrates used in this work were p-type and an n-type dopant was added to the melt to obtain an n-type silicon layer and compensate for the p-type doping.

3.1.4 LPE apparatus

A conventional sliding boat configuration (Astles, 1990) is used in this work. The instrument consists of a three zone furnace which is attached to a glove box used for loading substrates and growth materials. The glove box is filled with 5.5N N_2 gas and pressure regulators are used to maintain a constant inside pressure. A quartz tube connected to a gas and exhaust system is positioned inside the furnace. Inside

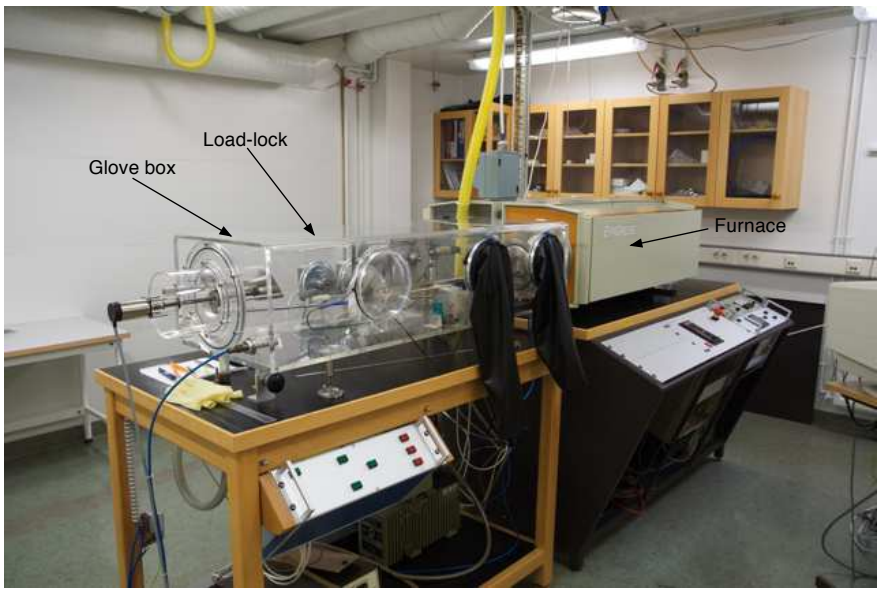


Figure 3.3: The LPE system used. To the left is the glovebox and to the right is the LPE furnace.

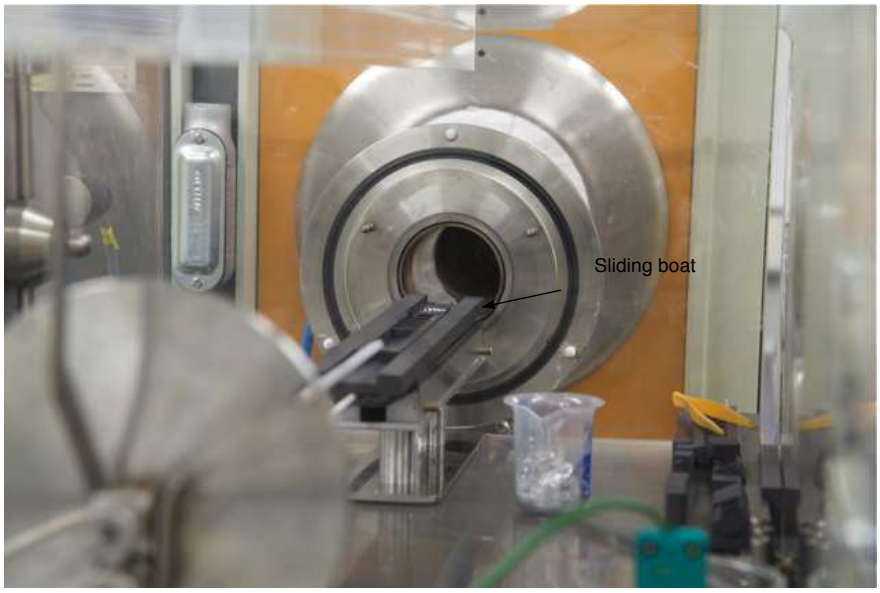


Figure 3.4: Inside the glovebox. In the process, the graphite boat is placed on top of the graphite slider.

the quartz tube is the graphite sliding boat system. The complete LPE system is shown in figure 3.3 and the sliding boat inside the glove box is shown in figure 3.4. The setup of the sliding boat and the crucibles is shown schematically in figure 3.5. A step motor is connected to a fork that the substrate is mounted into and is used to position the substrate under the crucibles containing the growth solution. Weight is put on top of the growth solution to ensure that it spreads over the substrate. The temperature inside the quartz tube is measured with a thermocouple and a standard PID temperature controller is used to regulate the temperature and allow control with a PC computer. A constant flow of 5N hydrogen, additionally purified to 7N by a palladium hydrogen cell is used to prevent oxidation of the substrate in the chamber.

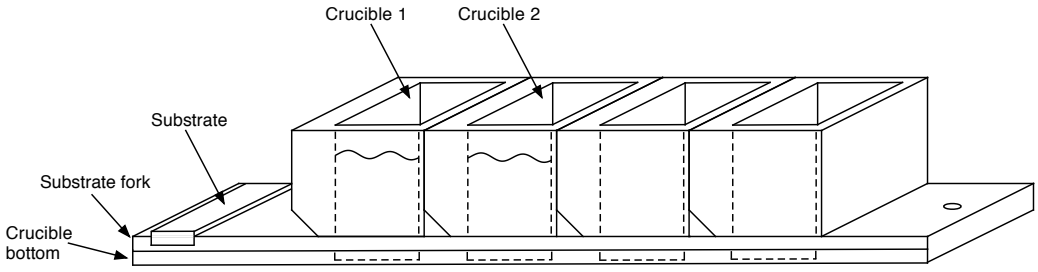


Figure 3.5: The sliding boat setup. The crucibles are confined within the crucible bottom and the substrate fork. The substrate is placed in the substrate fork and which can be positioned under each of the crucibles.

3.2 Hydrogenation of the as-grown silicon

Hydrogen can be used to passivate both donor and acceptor impurities in silicon (Pearton et al., 1992). Furthermore, it has been used effectively to reduce the defect concentration in poly-crystalline silicon by $10^{17}\,\mathrm{cm}^{-3}$ to a sub micron depth (Honda et al., 2005). The hydrogenation increases the minority carrier diffusion length (Darwiche et al., 2007) and is a low cost and efficient method to improve the electrical properties of silicon. Darwiche et al. (2007) studies the effects of hydrogenation on the chemical and electrical properties of poly-crystalline silicon surfaces. The main results were that the hydrogen concentration depends strongly on the power applied to the discharge, the exposure time as well on the gas concentration. The effective minority carrier diffusion length improved after the hydrogenation. They also showed that there exists an optimal exposure time for the hydrogen incorporation and thus minimal defect (dislocation or grain boundary) generation. The system used for hydrogenation in this work is an inductively coupled rf plasma discharge in the cylindrical configuration. A schematic of the setup is shown in figure 3.6. A quartz tube 38.3 mm in diameter and 245.2 mm long is connected to a vacuum pump system on the right. Ar and H_2 gas inlets are connected to mass flow controller for controlling the gas flow in the tube. The

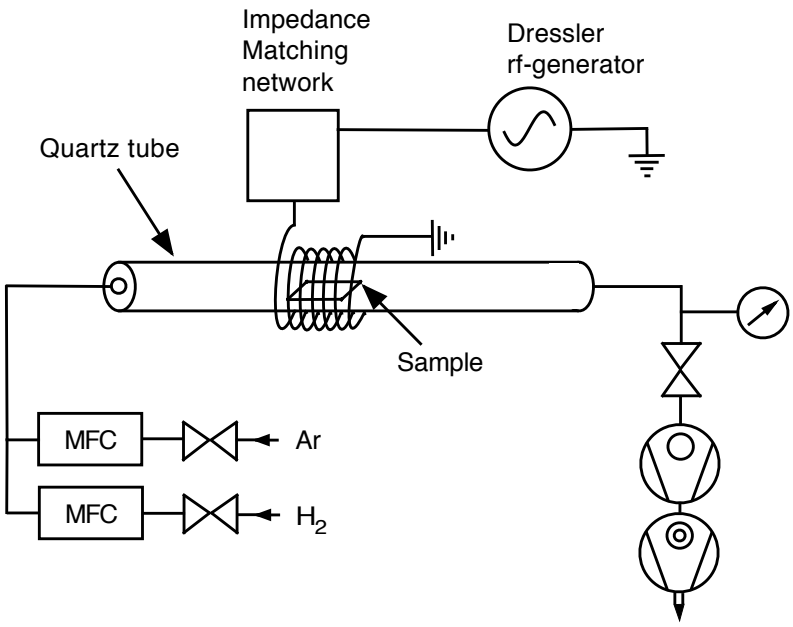


Figure 3.6: The setup used for hydrogenation of the grown samples. The sample to be hydrogenated is positioned inside the quartz tube, under the inductive coil.

quartz tube is placed inside an induction coil which is connected to an Dressler Cesar 136 rf-generator through an external matching network to optimize the power transfer. The operating frequency used for the discharge is 13.56 MHz.

The as-grown samples were hydrogenated for 40 minutes in an Ar/H_2 (1:1) mixture at a total pressure of 12 mTorr. The incident power was 80 W. Prior to the hydrogenation the native oxide film of the samples was removed with HF:DI water (1:20) in an ultrasonic bath for 1 minute.

3.3 Metal contacts on semiconductors

An ohmic contact is a metal-semiconductor contact that has a low contact resistance with the semiconductor material relative to the bulk or series resistance of the semiconductor. If the doping concentration in the semiconductor is low, then the

current transport is dominated by the thermionic-emission current. For higher doping concentrations, tunneling current dominates and the barrier width is narrow. An ohmic contact is a metal-semiconductor contact with a low barrier ($\phi_{\mathrm{B}} \leq kT$). For an n-type semiconductor, the barrier height is the difference between the metal work function ϕ_{m} and the semiconductor electron affinity χ

$$q\phi_{\mathrm{Bn}} = q\left(\phi_{\mathrm{m}} - \chi\right). \tag{3.3}$$

For an p-type semiconductor, the barrier height is

$$q\phi_{\mathrm{Bp}} = E_{\mathrm{g}} - q\phi_{\mathrm{Bn}} = E_{\mathrm{g}} - q\left(\phi_{\mathrm{m}} - \chi\right) \tag{3.4}$$

as the sum of the barrier heights is equal to the band-gap. For the barrier height to decrease, the metal work function must decrease. Traditionally, another method is used for making ohmic contacts. That involves creating a highly doped region and depositing a metal contact on top.

Ohmic contacts on n-type silicon are often made by evaporating an alloy of Au-Sb (0.1% Sb) or Ag on the grown film and then anneal at the eutectic temperature under an inert gas (Sze, 1981). Normally, after depositing the metal on the semiconductor, an annealing step would be required for the metal to diffuse into the semiconductor. In our case this would make the hydrogen diffuse from the junction and therefore it was avoided. Electrical contacts were made with two methods. One is based on melting a thin gold wire into the surface of the film to make an ohmic contact. The other method is based on making a mechanical bond with the surface by ultrasonic vibrations. The surface of the grown layer must be sufficiently smooth in order for a good contact to be made without interruption in the current flow (Peter et al., 2002).

3.4 Measurements of minority carrier lifetime

The lifetime of photo-generated excess minority carriers is one of the key parameters in solar-cell design (Mahan et al., 1979). In particular, the overall energy conversion efficiency of the solar cell depends on the minority carrier lifetime. If the charge carriers recombine before they reach the junction, they will not contribute to the current across the p-n junction. The minority carrier lifetime essentially describes how far the carriers go before they recombine. Methods used to measure the minority carrier lifetime include photoconductive decay, rf-photoconductive decay, microwave absorption and photoluminescence decay (Kazmerski, 1998). The method described here is a variation of the photoconductive decay method.

The lifetime of photo-generated carriers in solar cells can be estimated by using an open-circuit voltage (V_{OC}) technique (Mahan et al., 1979). This technique was first introduced by Gossick (1955). Excess minority carriers are introduced by creating a short pulse of forward current. By cutting off the current abruptly and analyzing the voltage decay curve, information on the minority carrier lifetime are obtained. Mahan et al. (1979) showed that these excess carriers could also be photo generated, that is, a pulse of light could be used to measure the carrier lifetime. This method would be more relevant to investigate material for operation as a solar cell and therefore it was used here.

The photoconductive decay curve that is obtained when illuminating the solar cell can be split up in to three regions as shown in figure 3.7 (Mahan et al., 1979). The first region corresponds to high-level injection of minority carriers, the second region corresponds to intermediate injection of minority carriers and the third region to low-injection condition. In both the first and second regions, the voltage depends linearly on time and in the third region there is an exponential dependence of the voltage with time.

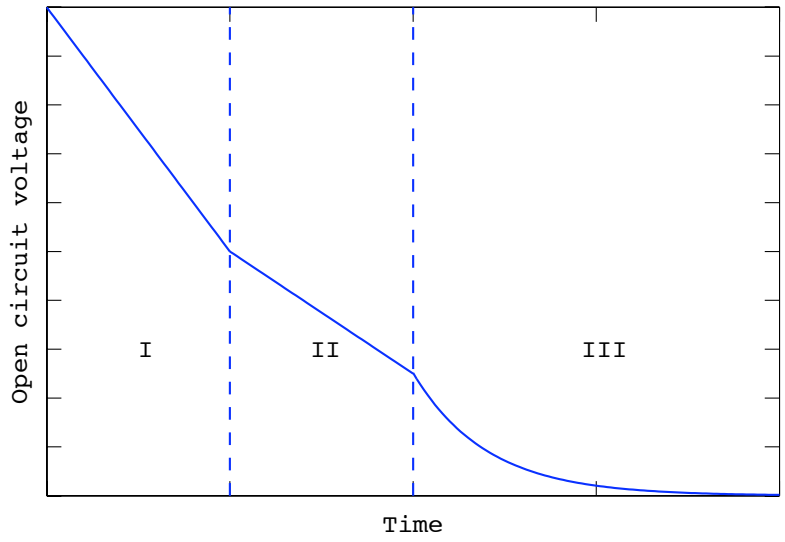


Figure 3.7: An open-circuit voltage decay curve. Redrawn from Mahan et al. (1979).

The lifetime can be calculated as (Bassett, 1969)

$$\tau = \frac{kT}{q} \left| \frac{dV_{\mathrm{OC}}}{dt} \right|^{-1} \tag{3.5}$$

where dV_{OC}/dt is the slope of the curve in region II. The measurements were made with an Agilent 54624-A oscilloscope accompanied with a LI-75A high input impedance low-noise preamplifier with differential inputs and an amplification of 100. The high-input impedance was needed to ensure that the solar cell was in open-circuit condition and not being loaded down. The sample was illuminated with a laser diode (635 nm) through a mechanical chopper to obtain a periodic signal. For light with wavelength of about 650 nm, the penetration depth into the silicon substrate is approximately 6 μm (Sze, 2002) and increases with increasing wavelength. Measurements of the open-circuit voltage were made with a Fluke 8842A multimeter.

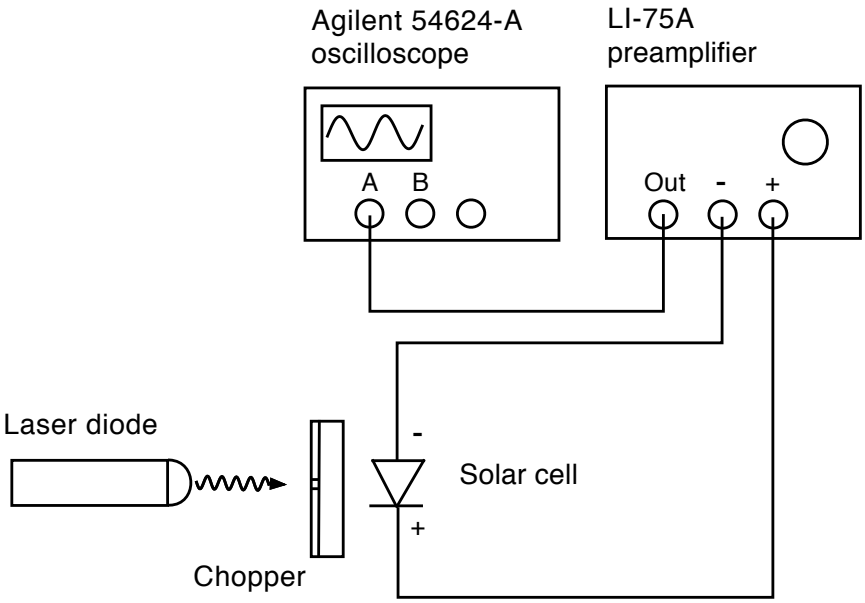


Figure 3.8: A schematic of the measurement setup. The laser diode illuminates the sample. The open-circuit voltage is measured with the preamplifier with differential inputs. The waveform is transferred from the oscilloscope to a PC computer.

3.5 Current-voltage measurements

The $I - V$ characteristics of the sample were obtained by measuring the current as a function of the voltage across the sample. The configuration of the measurement is shown in figure 3.9. The measurements were made with a Keithley 617 programmable electrometer and a computer was used to collect the data. Each step of the measurement is carried out by varying the voltage across the sample in steps of $\Delta V = 0.05\,\mathrm{V}$ and measure the current through the sample. The current range was $\pm 15\,\mathrm{mA}$. Prior to the measurement, ohmic contacts were evaporated on the sample with the method discussed in section 3.3. The sample was mounted in a tripod and aluminum wires were connected to the contacts with a Kulicke & Soffa ultrasonic bonding machine. The measurements were performed in dark room conditions at room temperature.

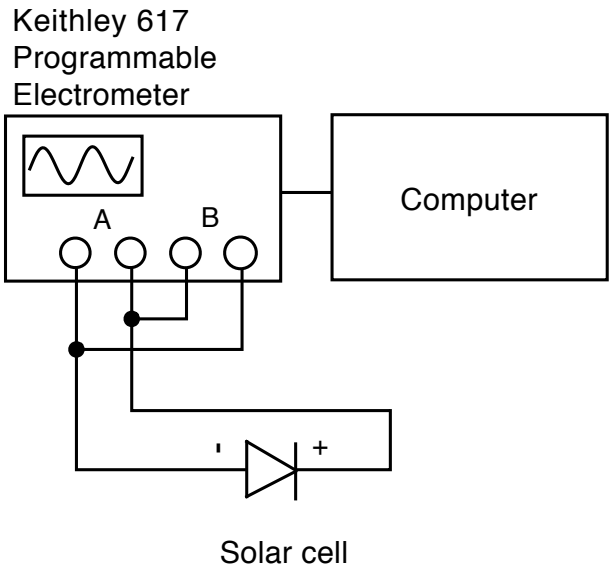


Figure 3.9: The setup of the $I-V$ measurement. Channel A measures the current through the sample and channel B is used to apply voltage on the diode.

3.6 Hall effect

Measurements of the carrier concentration and the electrical conductivity were made with a Hall and conductivity measurement system in the van der Pauw configuration (van der Pauw, 1958). The technique applies to semi-insulating samples that have arbitrary shape, uniform thickness and composition (van der Pauw, 1958). Figure 3.10 shows a uniformly doped layer, through which the current I_{x} flows and a magnetic field B_{z} that is applied across the layer at right angles to the direction of the current. This leads to an electric field E_{H} which is perpendicular to both the current and the magnetic field. This is the Hall electric field and is given by

$$E_{\mathrm{H}} = \frac{R_{\mathrm{H}} I_{\mathrm{x}} B_{\mathrm{z}}}{A} \tag{3.6}$$

where R_{H} is the Hall coefficient and A is the cross sectional area of the layer. If the width of the sample is w, $V_{\mathrm{H}} = E_{\mathrm{H}}w$ is the voltage across the layer, referred to as the Hall voltage and t is the thickness of the layers, then the Hall coefficient is given by

$$R_{\mathrm{H}} = \frac{t}{I_{\mathrm{x}}B_{\mathrm{z}}}V_{\mathrm{H}}. \tag{3.7}$$

The Hall coefficient R_{H} can be obtained by measuring V_{H} as a function of B_{z} where

$$V_{\mathrm{H}} = R_{\mathrm{H}}\frac{I_{\mathrm{x}}B_{\mathrm{z}}}{t} \tag{3.8}$$

is derived from equation (3.6). The polarity of the Hall coefficient gives directly the carrier type of the sample under measurement, but depends on how the sample is oriented in the measurement system (Ghandhi, 1983). For negative values of R_{H}, the sample is n-type, but for positive R_{H} the sample is p-type. The carrier

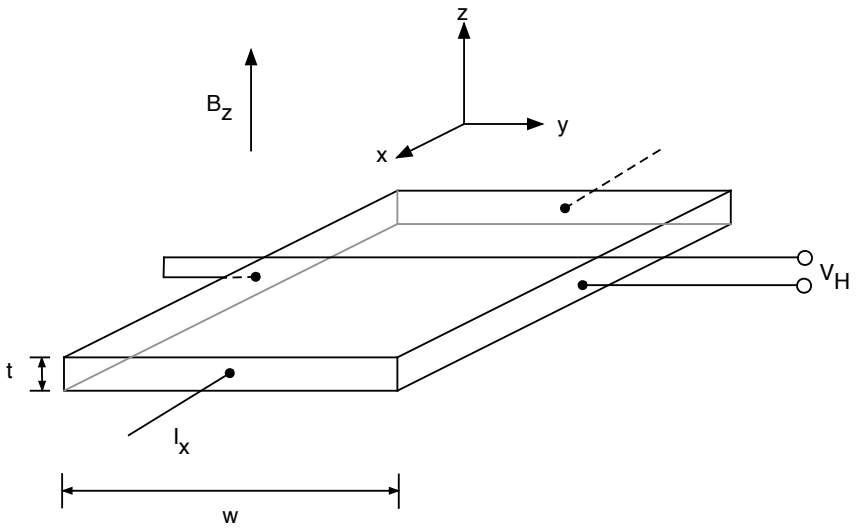


Figure 3.10: The configuration of the Hall measurement. The sample is of thickness t and width w. A static magnetic field B_{z} is applied in the z-direction and a current is applied in the x-direction. The Hall voltage V_{H} is measured across the sample in the y-direction.

concentrations are

$$n = -\frac{r_{\mathrm{H}}}{eR_{\mathrm{H}}} \tag{3.9}$$

$$p = +\frac{r_{\mathrm{H}}}{eR_{\mathrm{H}}} \tag{3.10}$$

where r_{H} is the Hall factor. The electrical conductivity of the sample is (van der Pauw, 1958)

$$\rho = \frac{\pi t}{\ln 2}\frac{R_{\mathrm{AB,CD}} + R_{\mathrm{BC,DA}}}{2} f(R) \tag{3.11}$$

where $R_{\mathrm{AB,CD}}$ is the resistance obtained by dividing the voltage applied between contacts A and B with the current entering contact A and leaving contact B and $R_{\mathrm{BC,DA}}$. The same applies to $R_{\mathrm{BC,DA}}$. $f(R)$ is a correction factor which is equal to unity when $R_{\mathrm{AB,CD}} = R_{\mathrm{BC,DA}}$. Once the conductivity and the carrier concentration are known, the Hall mobility is calculated as

$$\mu_{\mathrm{H}} = R_{\mathrm{H}}\sigma = r_{\mathrm{H}}\mu_{\mathrm{H}} \tag{3.12}$$

and it is assumed that $r_{\mathrm{H}} = 1$.

The measurement setup consists of a magnet in which the magnetic field can be varied from 0 T to 0.5 T, a Keithley 224 current source, a Keithley 2002 high-input impedance voltmeter, a Keithley 485 picoammeter and a custom made van der Pauw box.

Ohmic contacts were obtained by welding gold wires on a square sample of area 2 – 6 mm^2 by using a Biorad bonding machine.

3.7 SEM & AFM

In a scanning electron microscope (SEM) the surface of interest is scanned with an electron beam and the reflected (or back-scattered) beam of electrons is collected. SEM can provide information about surface topography, crystalline structure and chemical composition of a sample. It is a non-destructive method. An important advantage of SEM is the good contrast and easy preparation of samples. The surface must be electrically conductive as the incident electrons interact with the electrons on the surface of the sample. The sample is positioned in a high vacuum chamber to reduce the possibility of scattering of the electrons with the atmosphere. SEM offers magnifications that can range from 10 to at least 50000 diameters, a great depth-of-focus, compared with a maximum magnification of an optical microscope (1000×), and a limited depth of field. The large depth-of-focus of SEM is advantageous because then the roughness of the samples is not a limiting factor. The amount of depth-of-focus can be as much as 400 times greater than that of an optical microscope (Flegler et al., 1993). The resolution of the SEM is around 5 nm (Flegler et al., 1993).

Electrons created at a cathode are accelerated by a high voltage between the cathode and an anode. A magnetic lens system is used to create an electron beam 1-10 nm in diameter and forming an electron current of $10^{-10}-10^{-12}$ A on the surface. The electron current is commonly referred to as probe current. Apertures are used to increase the depth-of-focus and improve the angular resolution. A deflection coil system is used to raster scan the probe across the surface of the sample. The signal is detected, amplified and analyzed with a computer. Secondary electrons are easily collected with a photomultiplier and a positively biased collector grid. By detecting backscattered electrons the surface topography can be imaged at a lower magnification and has a better shadowing effect than the secondary electrons

(Reimer, 1985). The measurements were made with a LEO Supra 25 scanning electron microscope at the Innovation center of Iceland.

The atomic force microscope (AFM) is a high resolution scanning probe microscope used to investigate both insulators and conductors on an atomic scale (Binnig et al., 1986). The technique is based on scanning the surface of a sample with a microscale cantilever. The sample is positioned on top of a piezoelectric drive which allows for scanning in three dimensions. When the cantilever tip is near the surface, a variation in attractive forces between the electrons in cantilever and the sample lead to a deflection of the cantilever, according to Hooke's law. A laser beam is pointed towards the cantilever and detected by a photodiode. A deflection of the cantilever causes a variation in the current of the photodiode. An image of the surface is obtained by scanning the surface. The resolution of the AFM is in the range of 0.1 nm or less (Flegler et al., 1993). Furthermore, the roughness of surfaces can be estimated. The measurements were made with a PSIA XE-100 from Park Systems at the Innovation center of Iceland.

3.8 XRD

X-ray diffraction techniques are used to obtain information on the crystal structures of solids. A monochromatic X-ray beam is sent to the surface of a sample at a specific angle and the intensity of the scattered wave is measured. Laue proposed that if a crystal was composed of regularly spaced atoms which could act as scattering centers for X-rays and if the interatomic distance is comparable to the wavelength of the X-rays, then it should be possible to diffract X-rays by means of crystals (Cullity, 1978). The condition for diffraction to occur is referred to as Bragg's law. For fixed values of λ and d, there may be angles θ which diffraction can occur. The first order diffraction from planes of spacing d and the angle of the

diffracted X-rays θ are related by Bragg's law

$$\lambda = 2d \sin\theta. \tag{3.13}$$

Traditionally, a $2\theta - \omega$ configuration is used where the X-ray tube is stationary and the sample is rotated instead. There ω is equal to half the scattering angle (2θ). To analyze poly-crystalline thin films, a configuration can be used which is referred to as Grazing Incidence X-ray Diffraction (GIXRD) (Birkholz, 2006). Then the angle ω is very small compared with θ, or on the order of a few degrees. In this way, it can be ensured that the diffracted X-rays originate in the grown film, instead of the substrate, since the X-rays do not penetrate as deep when ω is small.

Experimentally, Bragg's law can be applied by using a monochromatic X-ray beam of a known wavelength λ and measure the intensity of the diffracted rays with a counter while varying θ. In this way the crystal planes can be identified and the spacing calculated.

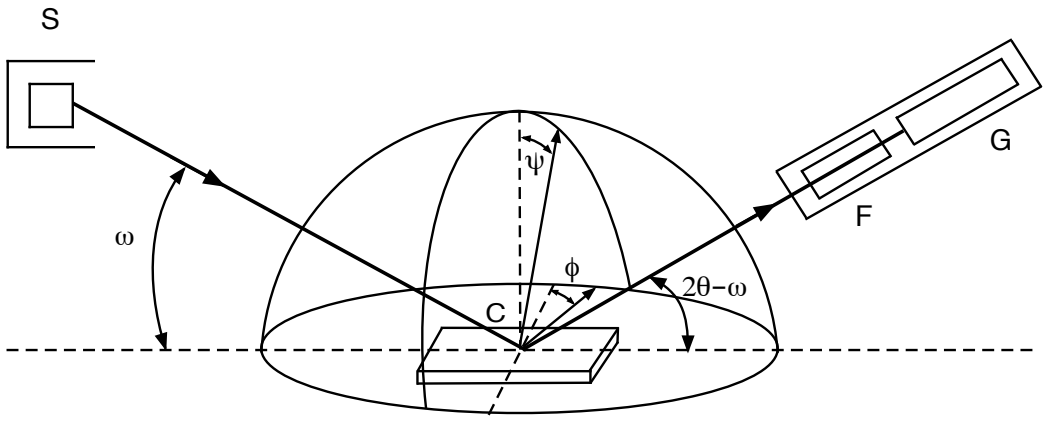


Figure 3.11: The diffractometer setup for XRD configuration. X-rays diverge from the X-ray source labeled with S. The X-rays are diffracted from the crystal C and converge at the slit F and from there enter the counter G. In the case of GIXRD, ω is very small compared with θ.

A basic setup of a diffractometer is shown in figure 3.11. X-rays diverge from the X-ray source labeled with S. The X-rays are diffracted from the crystal C and converge at the slit F and enter the counter G. In XRD, the angle between the horizontal plane of the sample and the beam is θ and 2θ with respect to a plane parallel to the source and the beam. In the $\theta - 2\theta$ configuration, the angle θ is often referred to as ω. In GIXRD, ω is very small when compared to θ. Additionally, the sample can be rotated around the center of a vertical axis of the sample holder, where the angle between the vertical axis of the sample holder and the vertical axis of the diffractometer is ϕ. The sample can also be rolled around a horizontal axis through the sample, where the angle Ψ is between a vertical axis through the sample holder and a vertical axis through the sample.

If the grains have a preferential crystallographic direction the material is said to have texture. The crystal structure and the crystal planes can be identified by comparing the Bragg angle θ_{B} and d with table values.

The measurements were made with a Panalytical X'pert PRO diffractometer and CuK_{α} (0.154 nm) radiation was used.

Chapter 4

Results and discussion

Film growth by LPE was carried out on three types of substrates, a semi-insulating (SI) single-crystalline silicon, p-type single-crystalline silicon and an MG-Si poly-crystalline silicon. The semi-insulating single-crystalline silicon substrate is used for determination of the carrier concentration in the grown film. The p-type single-crystalline silicon substrate is used as a reference sample for comparison of the electrical properties of the grown films. The substrate preparation is described in section 4.1 and the growth parameters in section 4.2. The grown samples and substrates were characterized with respect to crystallinity and morphology as discussed in section 4.3. The electrical properties of the grown films are discussed in section 4.4.

4.1 Substrate preparation

A poly-crystalline metallurgical grade silicon (MG-Si) substrate was obtained by slicing an MG-Si rock/chunk of grade 441 (0.40%wt of Fe and Al and 0.10%wt of Ca), supplied by Bit Metals BV, with a low speed diamond saw (SBT model

650). Afterwards the substrate of dimensions $9 \times 18\,\mathrm{mm}^2$ was polished roughly with sandpapers of different roughness to a thickness of $1.0 \pm 0.1\,\mathrm{mm}$. A Jean Wirtz TG-250 polishing machine was used to polish the substrate further. The substrate was fastened onto a rotating holder and pressed against a rotating disc covered with a velvet cloth. The disc rotated in a direction opposite to the holder. A water suspension of alumina with particle size $\leq 0.1\mu$m was used as an abrasive. Turpentine was used to remove the wax remains after the polishing process. The single-crystalline silicon substrates together with the sacrificial silicon were etched in DI:HF (1:1) for 4 minutes in an ultrasonic bath in order to remove native oxide. The etchant was rinsed off in de-ionized (DI) water in an ultrasonic bath for 5 minutes. Prior to entering the load-lock of the LPE system, the substrates were dipped in DI:HF (1:1) for a few seconds, rinsed in DI water and dried with N_2 pressurized gas. This was done to ensure an oxide free surface before growth. In the case of the MG-Si substrate, the acid etching step was omitted due to the porous nature of the substrate and possible incorporation of the etchant into the substrate. Then the substrates, the sacrificial silicon (solute) and the indium were cleaned in trichloroethylene, acetone and isopropanol respectively for 4 minutes each in an ultrasonic bath. A rinse in DI water in an ultrasonic bath followed.

4.2 LPE growth parameters

Figure 3.5 shows the setup of the crucibles for the LPE growth. The substrate is positioned on the left and can be dragged to the right and placed under any of the crucibles, as can be visualized from figure 3.5. In the case of the single-crystalline substrate, crucible 1 contains melted gallium that is approximately 80% saturated with silicon. In the case of the MG-Si substrate, crucible 1 contains melted gallium that is approximately 95% saturated with silicon. Crucible 2 contains a Ga/In

solution in weight proportions 3:1. When the substrate is positioned under crucible 1 at the growth temperature, the gallium melt dissolves a part of the substrate which in turn aims for better wetting of the substrate. The Ga and In atoms both have a valence of 3 and thus act as acceptors in silicon. Arsenic donor dopant is provided by GaAs that is dissolved in the melt. Only a trace amount of GaAs is required to compensate for the acceptor doping from both the Ga and In due to the much higher segregation coefficient of As (Sze, 2002). The doping concentration is controlled by the amount of GaAs added. Crucible 3 is empty and has the role of removing the remains of the melt from the surface of the substrate. Saturation of the solvent was carried out for 90 minutes at the growth temperature (900°C) under reducing hydrogen flow. The substrate was then moved under the melt in crucible 1 and kept there for 5 seconds. Subsequently it was moved under crucible number 2 and kept there for another 90 minutes. The sample was then ramp cooled with a cooling rate of 1°C/min, from 900°C to 860°C. The hydrogen flow was maintained at 100 ml/s during the growth and until the sample temperature reached 750°C. The substrate was moved from the growth melt under an empty crucible at 860°C. After the growth the gallium residue was cleaned off by immersing the sample in warm isopropanol (IP) and wiping the melt off with cotton pin, followed by a rinse in a HCl:DI water (1:10) solution in an ultrasonic bath for 5 minutes.

4.3 Growth characterization

The crystallinity of the substrates and films was explored by X-ray diffraction (XRD). Then the substrates and films were characterized with respect to morphology using a scanning electron microscope (SEM) and an atomic force microscope (AFM).

Crystallinity

Information regarding the crystal structure of the substrates and grown films was obtained using XRD and GIXRD. The measured spectra were filtered using a Blackman filter. For the single-crystalline substrate and films, a $2\theta - \omega$ scan was done. For the grown films and the MG-Si substrate, the measurements were made using GIXRD. The sample was rotated from $\phi = -180°$ to $\phi = 180°$ at each of the known silicon diffraction peaks and a 2θ scan was made.

The XRD spectrum of the single-crystalline substrates, prior to growth is shown in figure 4.1, marked with (a). The existence of single high intensity peak at $2\theta = 69.12°$ confirms that the substrate is single-crystalline. This corresponds to a diffraction from the [400] plane. Additionally, there is a peak at $2\theta = 136.45°$ which corresponds to a diffraction from the [533] plane in silicon. The peak at $2\theta = 116.64°$ can possibly be attributed to a surface oxide on the substrate. For the films grown on single-crystalline substrates, the crystallinity is good and for

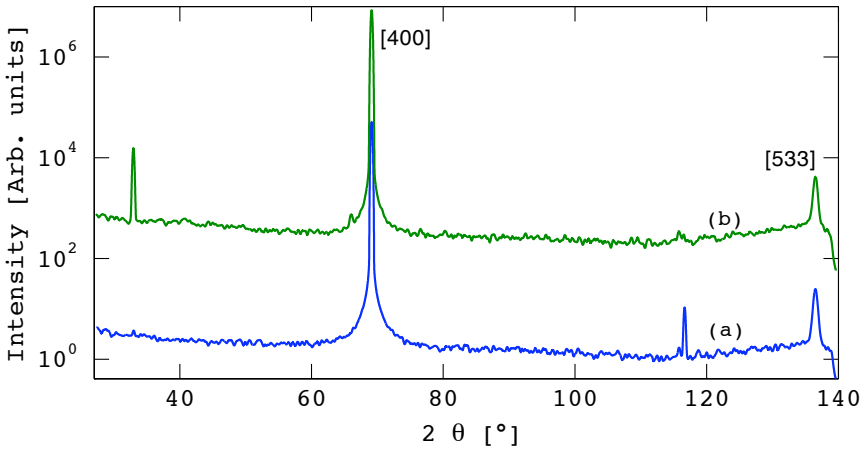


Figure 4.1: The measured (a) XRD spectrum of a single-crystalline substrate and (b) XRD spectrum of a silicon thin film grown with LPE on a single-crystalline substrate at 900 °C using a Ga/In solvent. The curves are shifted for clarity.

comparison the measured XRD spectrum is shown in figure 4.1, marked with (b). A peak was observed at $2\theta = 69.11°$ which corresponds to a diffraction from the [400] plane. The diffraction peak at $2\theta = 32.97°$ can possibly be attributed to an oxide residing on the surface and the diffraction peak at $2\theta = 136.51°$ corresponds to a diffraction from the [533] plane in silicon. A GIXRD scan was performed for the grown film and no diffraction peaks were observed as expected.

GIXRD spectra of the MG-Si substrates, prior to growth are shown in figure 4.2. There are three spectra taken at: (a) $\phi = -103.5°$, (b) $\phi = -70.8°$, (c) $\phi = 4.12°$. Those ϕ positions were chosen as the highest diffraction peaks existed there. It can be seen that the peak with the highest intensity is at $2\theta = 56.09°$, which corresponds to diffraction from the [311] plane which indicates that the MG-Si substrate was poly-crystalline and textured with preferentially oriented grains in the [311] direction.

GIXRD spectra of the films grown on the MG-Si substrates, are shown in figure 4.3. There are five spectra taken at: (a) $\phi = -93.8°$, (b) $\phi = -62.5°$, (c) $\phi = 0.3°$, (d) $\phi = 27.0°$, (e) $\phi = 46.2°$. Those ϕ positions were chosen as the highest diffraction peaks existed there. The peak with the highest intensity is at $2\theta = 56.04°$, which corresponds to diffraction from the [311] plane. That indicates that the films grown on the MG-Si substrate were poly-crystalline and textured with grains preferentially oriented in the [311] direction.

In the case of the MG-Si substrates, the size of the grains was visually inspected and was on the order of mm. Because of the large grain size, the XRD method cannot be used to determine the grain size. When the MG-Si chunks used as starting materials are sawed into substrates, it is very difficult to ensure that the orientation of all of the substrate is the same. Consequently, the substrates used in the growth process are not identical. In the case of the MG-Si grown film, it can be

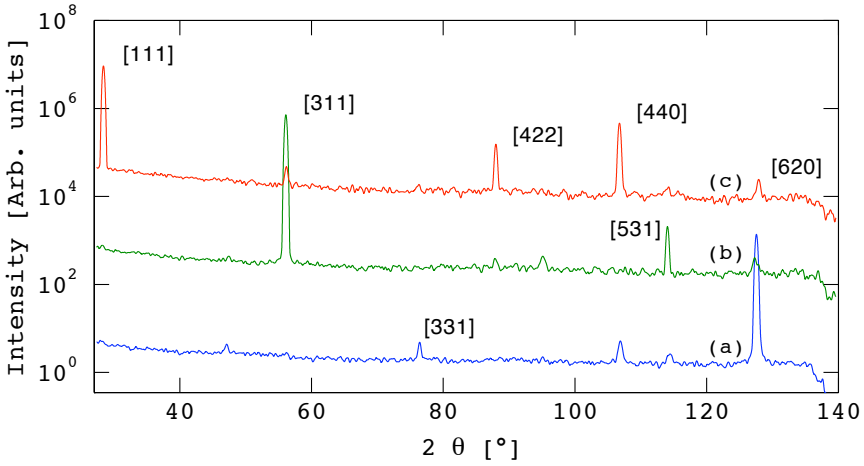


Figure 4.2: The measured GIXRD spectra of a MG-Si substrate for 3 different ϕ positions: (a) $\phi = -103.5°$, (b) $\phi = -70.8°$, (c) $\phi = 4.12°$. The curves are shifted for clarity.

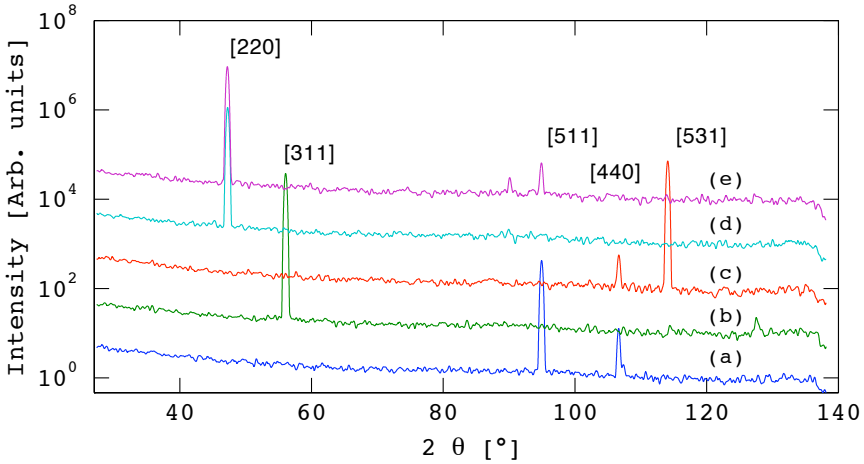


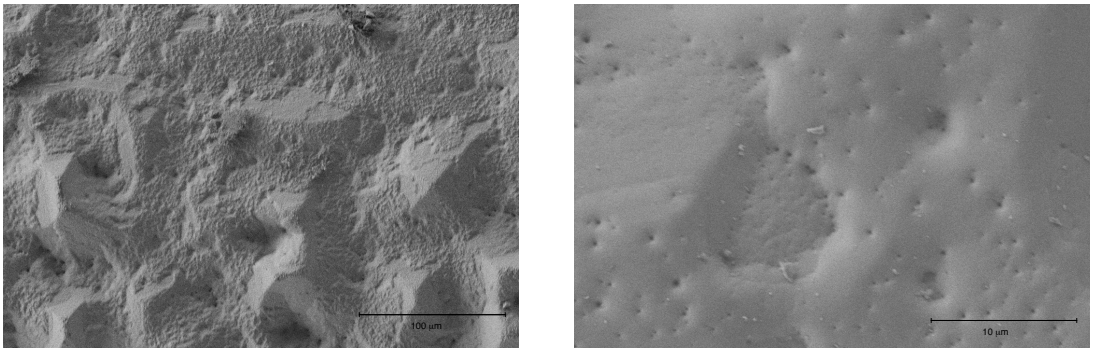
Figure 4.3: The measured GIXRD spectra of a film grown with LPE on an MG-Si substrate at 900 °C using a Ga/In solvent on a MG-Si substrate. Five different ϕ positions were measured: (a) $\phi = -93.8°$, (b) $\phi = -62.5°$, (c) $\phi = 0.3°$, (d) $\phi = 27.0°$, (e) $\phi = 46.2°$. The curves are shifted for clarity.

seen that there are fewer diffraction peaks present in the grown film as compared to the substrate. This indicates that the crystallinity of the films grown on MG-Si is better than for the substrate itself.

Morphology

Figures 4.4 (a) and 4.4 (b) show SEM micrographs of silicon thin films grown with LPE on a single-crystalline substrate at 900 °C with a cooling rate of 1.0 °C/min. The films grown on the single-crystalline substrates were smooth with ripples on the surface. The substrate coverage by the grown film on the substrates was dependent on the chemical treatment of the substrate prior to the growth. In some cases where insufficient coverage was observed, the presence of native oxide may have been the cause. In the case of the single-crystalline substrate, this was mostly avoided by chemical etching prior to growth. Due to the porous nature of the MG-Si substrate it became difficult to remove the residues of the etchant and therefore the wet etching step was omitted in these cases. Instead, the MG-Si substrates were polished prior to growth which eliminated the native oxide.

It can be shown that the film shown in figure 4.4 (a) is very rough on a microscopic scale. A probable cause is the melt-back step in the growth process. The amount of melt-back was higher for the films grown on single-crystalline substrates than for the films grown on the MG-Si substrates and therefore more of the sur-



(a) **(b)**

Figure 4.4: SEM micrographs of a silicon thin film grown with LPE on a single-crystalline substrate at 900 °C using a Ga/In solvent. Figure (a) shows a rough surface of the film. Figure (b) shows a smoother part of the film on a smaller scale.

face was dissolved in the melt. When the silicon surface did partially dissolve in the melt, a pyramidal like structured surface was obtained. The grown film has a similar contour as of the surface it was grown on. A smoother surface can possibly be obtained by decreasing the amount of melt-back. The film shown in figure 4.4 (b) shows a smoother surface of a film grown at the same conditions. This shows that smooth regions exist in between the rougher regions.

The RMS surface roughness was measured by AFM and visualized on the micrographs shown in figure 4.5. Figure 4.5 (a) shows a surface area of 1600 μm^2 and the RMS roughness is 702 nm for the whole area. Figure 4.5 (b) shows an area of 100 μm^2 and the RMS roughness for the whole area is 248 nm. The surface shown in figure 4.5 (a) is clearly rougher and figure 4.5 (b) shows a portion of the surface in the lower left corner of figure 4.5 (a).

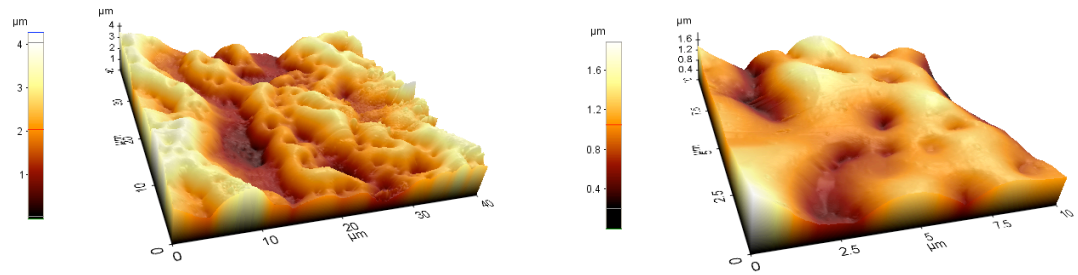


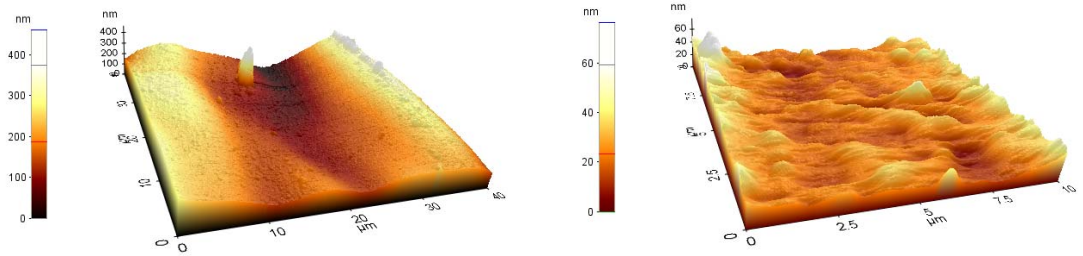
Figure 4.5: AFM micrographs of a silicon thin film grown with LPE on a single-crystalline substrate at 900 °C using a Ga/In solvent. Figure (a) shows a rough area and figure (b) shows the smoother area in the left lower corner of figure (a).

The AFM micrographs for the MG-Si samples are shown in figure 4.6. Figure 4.6 (a) shows an area of 1600 μm^2 and the RMS roughness is 68.9 nm for the whole area, excluding the spike visible in the figure. Figure 4.6 (b) shows an area of 100 μm^2 and the RMS roughness for the whole area is 7.6 nm. The ripples can also be visualized in the AFM micrograph in figure 4.6 (a). An estimate of the thickness of

the grown film was made by calculating the amount of silicon that was deposited on the substrate from the melt. The thickness was estimated to be $20.0 \pm 0.4\,\mu$m for the grown films.

Figure 4.7 shows a SEM micrograph of a polished MG-Si substrate. Fissures resulting from the metallurgical process are clearly visible. Figures 4.9 - 4.10 show SEM micrographs of silicon thin films grown with LPE on a MG-Si substrate at 900 °C with a cooling rate of 1.0 °C/min. Wave-like ripples can be formed on a rather smooth surface as seen in figure 4.8. The ripples occur because of deviations from the optimized growth conditions (Scheel, 2007). Figure 4.9 (a) shows a rough area of the film in which a grain boundary is visible. Figure 4.9 (b) shows the same area with a higher magnification. Figure 4.10 (a) shows a part of a surface defect or a grain boundary. Figure 4.10 (b) shows a smooth part of the film within a single grain and remains of the Ga solvent.

The films grown on the MG-Si substrates had a much rougher texture on a macroscopic scale compared to the films grown on the single-crystalline substrates. This was expected as the crystal structure of the film imitates the crystal structure of the substrate. It was striking that the films grown on single-crystalline substrates



(a) **(b)**

Figure 4.6: AFM micrographs of a silicon thin film grown with LPE on a MG-Si substrate at 900 °C using a Ga/In solvent. Figure (a) shows a wavy, but smooth surface. Figure (b) shows the same surface at a higher magnification.

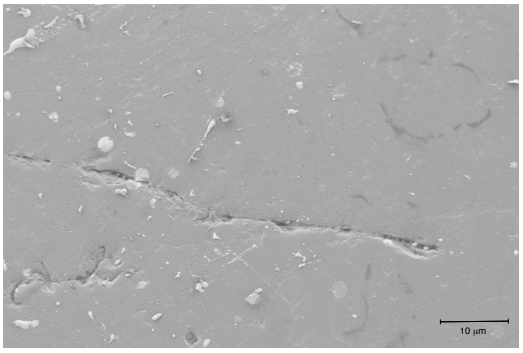


Figure 4.7: A SEM micrograph of a polished MG-Si substrate.

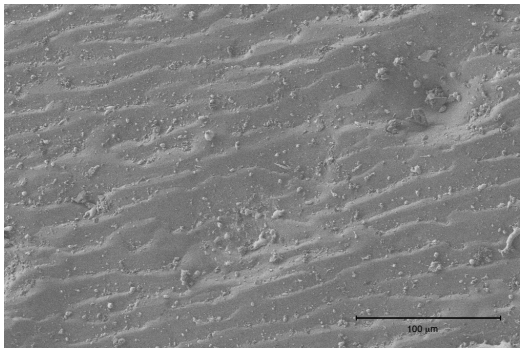
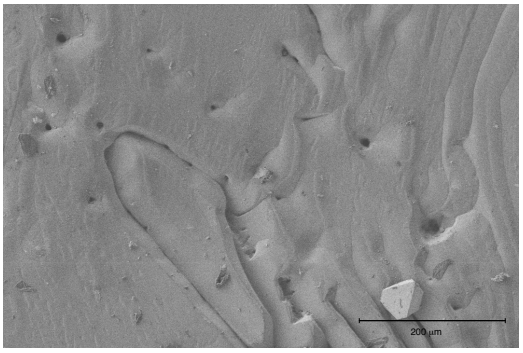
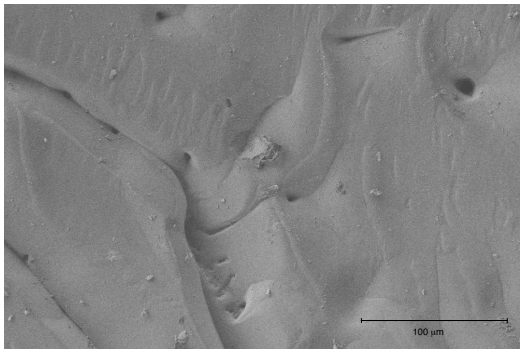


Figure 4.8: A SEM micrograph of a silicon thin film grown with LPE on a MG-Si substrate at 900 °C using a Ga/In solvent.



(a)

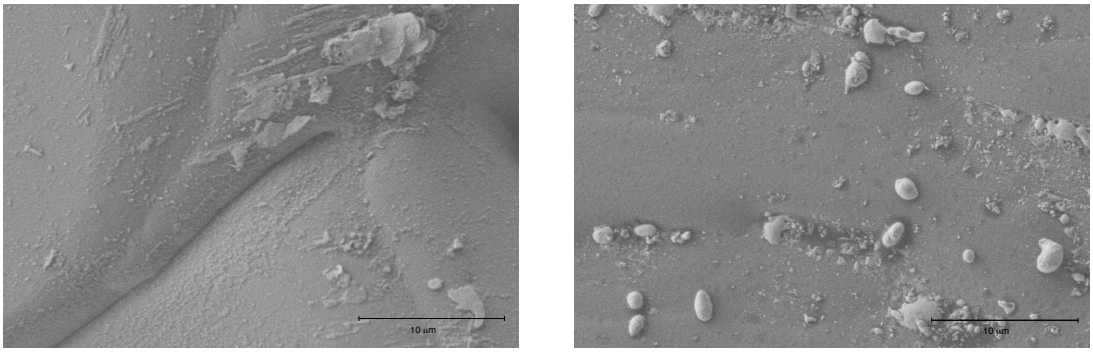


(b)

Figure 4.9: SEM micrographs of a silicon thin film grown with LPE on a MG-Si substrate at 900 °C using a Ga/In solvent. Figure (a) shows a rough area and a grain boundary is visible. Figure (b) shows a higher magnification of the area.

were in fact rougher on a microscopic scale, but that can be attributed to bad wetting of the substrate. Any surface defects such as fissures would act as preferable nucleation sites for film growth.

Kopecek et al. (2000) report on LPE growth on single-crystalline silicon substrate grown at 920 °C with a Ga/In solvent. They obtain a fairly smooth surface, similar to the ones observed in this current work, free of pyramidal structures, with a growth rate of 3 μm/h. Hötzel et al. (2000) grow thin film silicon layers



(a) **(b)**

Figure 4.10: SEM micrographs of a silicon thin film grown with LPE on a MG-Si substrate at 900 °C using a Ga/In solvent. Figure (a) shows a part of a surface defect or a grain boundary. Figure (b) shows a smooth part of the film within a single grain and remains of the Ga solvent.

with LPE using an indium solvent on an UMG-Si substrate. They obtain very smooth surfaces with growth rates of 30 μm/h. The growth rate in this current work was estimated as 60 μm/h based on the cooling rate and phase equilibria. Higher growth rates of 120 – 240 μm/h resulted in rougher surfaces.

4.4 Electrical characterization

The carrier concentration and the mobility of the charge carriers in the substrates and the films was determined by Hall and conductivity measurements. Furthermore, the $I - V$ characteristics, the open-circuit voltage and the minority carrier lifetime was measured.

Hall measurements

Hall measurements were made on grown films on semi-insulating silicon substrates and for the three types of substrates used for growth. This was done to determine the amount of dopant required for an appropriate carrier concentration in

the grown film. An overview of the results is given in table 4.1. The MG-Si substrate is highly p-doped with carrier concentration of $\sim 10^{18}\,\mathrm{cm}^{-3}$ and mobility of $55\,\mathrm{cm}^2/\mathrm{Vs}$ which is only half of that of a typical p-type single-crystalline silicon at a doping concentration of $10^{18}\,\mathrm{cm}^{-3}$ (Sze, 2002). The amount of dopant (GaAs) needed was found in a systematic way. Due to the small size of the weighted piece of dopant it was very difficult to precisely control its concentration in the grown film. It was found that approximately 2 mg of GaAs in 4 g of metal solvent gave $6 \times 10^{18}\,\mathrm{cm}^{-3}$ free electrons in the grown film. The carrier concentration in the film grown on the semi-insulating substrate is reduced by an order of magnitude by hydrogenation from $6.2 \times 10^{18}\,\mathrm{cm}^{-3}$ for as grown film to $3.3 \times 10^{17}\,\mathrm{cm}^{-3}$ for the hydrogenated film. For a comparison, a carrier concentration of $\approx 10^{17}\,\mathrm{cm}^{-3}$ can be considered appropriate for photovoltaic applications (Kopecek et al., 2000). Furthermore, the mobility of the grown film almost doubles with hydrogenation from $60\,\mathrm{cm}^2/\mathrm{Vs}$ to about $118\,\mathrm{cm}^2/\mathrm{Vs}$. It is assumed that when the semi-insulating substrate is used, all of the conductivity measured is due to the grown film. The validity of the assumption can be seen from table 4.1 by comparing the products of the mobility and the carrier concentration for each sample. It can be seen that this product is lower for the semi-insulating substrate when compared with the other substrates.

Table 4.1: The results from the Hall and conductivity measurements at room temperature on the electrical properties of the substrates and the thin films.

Sample	Mobility [$\mathrm{cm}^2/\mathrm{Vs}$]	Resistivity [$\Omega - \mathrm{cm}$]	Carrier conc. [cm^{-3}]
Substrates			
SI-Si	1625	6.26×10^3	$n = 6.1 \times 10^{11}$
p-Si	342	9.79	$p = 1.9 \times 10^{15}$
MG-Si	55	1.11×10^{-1}	$p = 1.0 \times 10^{18}$
Grown films			
LPE SI-Si	60	1.67×10^{-2}	$n = 6.2 \times 10^{18}$
LPE SI-Si (H_2)	118	1.60×10^{-1}	$n = 3.3 \times 10^{17}$

$I-V$ measurements

The current-voltage ($I-V$) characteristics of the grown samples are shown in figures 4.11 (a) and 4.11 (b) for both the as grown as well as hydrogenated samples. An overview of the deduced parameters is given in table 4.2. The improvement of the $I-V$ characteristic of the single-crystalline samples by the hydrogenation is clearly visualized. For an n-type film on a p-type single-crystalline substrate, the forward threshold voltage decreased from 2.25 V to 0.75 V upon hydrogenation and the reverse breakdown voltage increases from -1.20 V to $<$ -10 V. The ideality factor decreases from 5.9 to 2.7 upon hydrogenation. For an n-type film on an MG-Si substrate, the forward threshold voltage increases from 0.1 V to 0.50 V with hydrogenation and the reverse breakdown voltage increases from -0.15 V to -1.25 V. Here however, the ideality factor increases from 3.0 to 4.3 upon hydrogenation. There is not a significant difference in the ideality factor values for the MG-Si samples. The observed difference in forward voltage for the single-crystalline samples can be due to ohmic losses in the contacts made to the layer.

The difference in forward voltage and breakdown voltage for the MG-Si samples can be attributed to the passivation of defects by the hydrogenation. It is possible

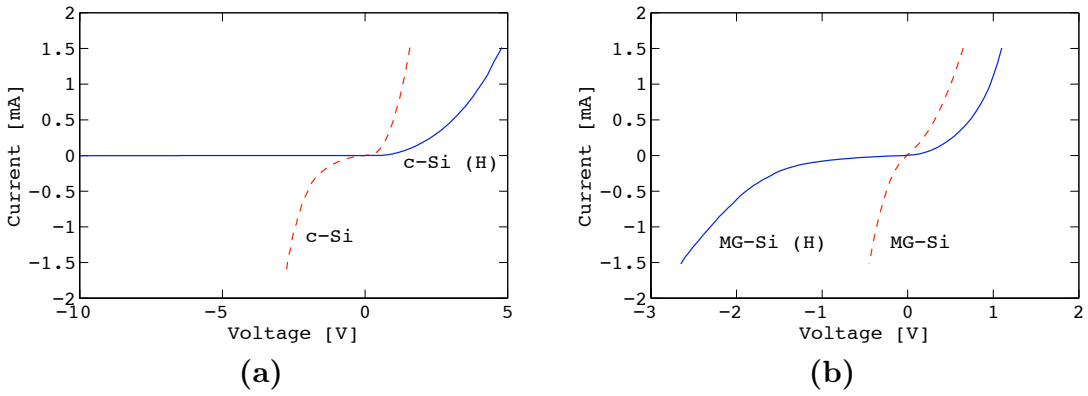


Figure 4.11: The $I-V$ curves measured for the grown films on (a) the single-crystalline substrate and (b) the MG-Si substrate, before and after hydrogenation.

Table 4.2: The results from the $I - V$ measurements at room temperature and at dark conditions.

Sample	Forward voltage [V]	Rev. breakdown voltage [V]	Ideality factor
p-Si substrate	2.25	< -10.00	5.9
p-Si substrate (H_2)	0.75	-1.20	2.7
MG-Si substrate	0.10	-0.15	3.0
MG-Si substrate (H_2)	0.50	-1.25	4.3

that the hydrogen does not diffuse far enough to reach the junction and therefore there is a higher concentration of hydrogen near the surface of the grown film. This could influence the contact made to the surface of the film and affect the $I - V$ characteristic. A perfect diode has an ideality factor of 1 but a diode having an ideality factor equal to 2 is considered to be poor. These values of around 6 are obviously too high to be considered a good measure of the quality of the diode.

Open-circuit voltage measurements

The open-circuit voltage is a first indication of the quality of the grown layer and the p-n junction. Table 4.3 gives overview of the measured open-circuit voltage. The open-circuit voltage of an as-grown film on an single-crystalline silicon substrate is 120 mV. The open-circuit voltage increases to 515 mV upon hydrogenation. The open-circuit voltage for the as-grown film on the MG-Si substrate is very low, or in the range 10-50 mV. Upon hydrogenation, the highest measured open-circuit voltage for the MG-Si sample was 307 mV, which is more than half of the highest measured open-circuit voltage for the film grown on the single crystalline silicon substrate. Regarding the MG-Si samples, the substrate is impure and some impurities might have made their way into the melt during the partial dissolution of the substrate. Consequently some of the impurities may have got incorporated into the film during growth with detrimental effects on the photovoltaic properties.

For the MG-Si samples, the response to incident light depended strongly on the position of the electrical connection to the surface. This can be due to variations in doping concentration and existence of recombination centers due to the impurities. There was a less dependence on the position of contacts in the case of the single-crystalline samples. The surface was much smoother and solvent inclusions are likely to be a less of a problem there. Possible reasons for lower open-circuit voltage are solvent inclusions and high contact resistance to the sample. These measured values can be compared to the results obtained by Ciszek et al. (1993) who measured an open-circuit voltage of 536 mV for an LPE grown sample on a cast MG-Si substrate using an Al solvent. A lower open-circuit voltage was measured when grown from an Cu solvent. They mention that a probable cause for the low open-circuit voltage were solvent inclusions in grain boundaries. The substrate they use is of higher quality though and it cannot be expected that we obtain the same measured values as they do. Peter et al. (2002) measured an open-circuit voltage of 597 mV for an LPE grown silicon on UMG-Si substrate using an In solvent at 990°C. Low shunt resistances can be caused by holes or cavities in the grown layer. The probability of the occurrence of the holes can be reduced by lowering the growth rate. Consequently, smoother layers are obtained (Hötzel et al., 2000).

Minority carrier lifetime measurements

The measured photoconductive decay curves for the single-crystalline and multi-crystalline samples are shown in figure 4.12. With reference to the photoconductive decay curve in figure 3.7, region II can be identified and the minority carrier lifetime can be calculated from the slope of the curve, according to equation (3.5). An overview of the results is given in table 4.3.

Table 4.3: Results from measurements of the open-circuit voltage and the minority carrier lifetime at room temperature.

Substrate type	Open-circuit voltage [mV]	Minority carrier lifetime [μs]
c-Si	120	4.9
c-Si (H_2)	515	11.0
MG-Si	$10 - 50$	-
MG-Si (H_2)	307	5.3

For the films grown on the single-crystalline substrates, the measured minority carrier lifetime is 4.9 μs. After the hydrogenation, the minority carrier lifetime has increased to 11.0 μs. For the grown films on the MG-Si substrates, the minority carrier lifetime was not measurable. After hydrogenation the minority carrier lifetime was measured 5.3 μs. As expected, the minority carrier lifetime is higher in the film grown on the single crystalline substrate. In both cases the hydrogenation

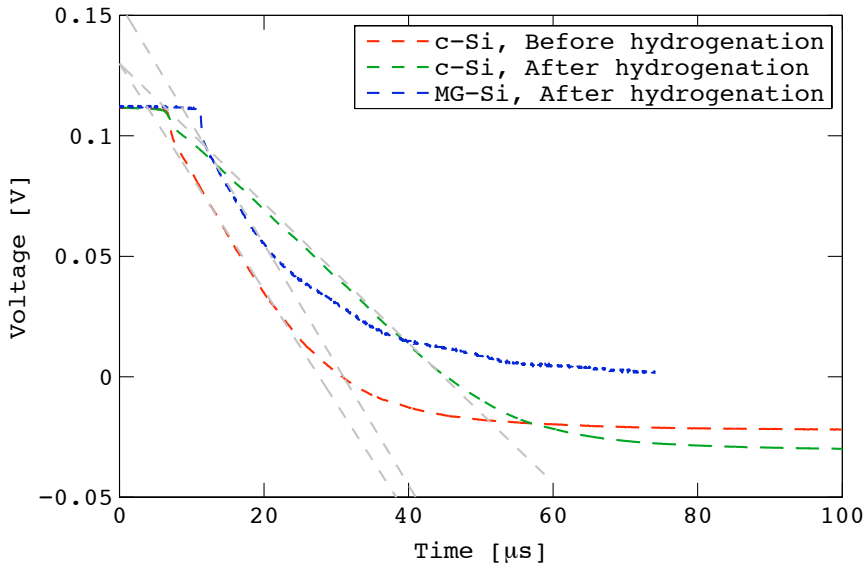


Figure 4.12: The measured open-circuit voltage decay curves for the as-grown and hydrogenated thin films grown on single-crystalline substrates and the hydrogenated films grown on MG-Si substrates. Three dashed lines are visible that fit to the linear region of each curve.

increases the minority carrier lifetime due to passivation of defects and reduced recombination activity of defects in the material. The photoconductive decay curve was not measurable for the as-grown film on MG-Si and we can assume that the lifetime was much lower in that case and the minority carriers would have recombined with the majority carriers before reaching the junction. Our values are similar to the values of Mahan et al. (1979) who measured the minority carrier lifetime of various commercially available solar cells with the photoconductive decay method. The measured lifetime was in the range of $5 - 25\,\mu$s. More recently, Kopecek et al. (2000) measured minority carrier lifetime of $14.7\mu s$ in an LPE grown layer from an Ga/In solvent on a single-crystalline silicon substrate.

It has been pointed out that by lowering the growth temperature, it can be expected that the minority carrier lifetime increases as reported by Satoh et al. (2005). They measured the minority carrier lifetime over a growth temperature range of 500-900°C and the result was that the minority carrier lifetime decreased drastically when the growth temperature was higher than 800°C.

Chapter 5

Conclusion

It has been shown that it is possible to obtain a p-n junction by growing thin film silicon on a MG-Si substrate by liquid phase epitaxy and subsequent hydrogenation. Additionally, an open-circuit voltage of 307 mV was measured for hydrogenated thin films grown on MG-Si, compared with 515 mV measured for hydrogenated thin films grown on single-crystalline substrates. Hydrogenation is a crucial factor in obtaining an active device for the case of the MG-Si substrate, or increasing the open-circuit voltage by a factor of 4 in the case of the single-crystalline substrate. The measured minority carrier lifetime also increased significantly by hydrogenation. The metallurgical-grade silicon (MG-Si) substrate has a potential of being used as low-cost alternative to crystalline substrates. It is very likely though, that the efficiency is being traded for cost.

Future tasks for this project are to measure the efficiency of the solar cell using standard methods as well as to characterize the samples further with respect to defects and impurity content in the grown films that can affect the carrier transport. Methods such as Secondary ion mass spectrometry (SIMS) and C-V profiling can

give valuable information regarding this. Furthermore, we plan to increase the size of the grown samples.

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