ORKUSTOFNUN
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SPRUNGUMÆLIR VIÐ LEIRHNJÚK

Hefti II: Viðaukar D-K

Einar Hrafnkell Haraldsson
Sverrir Hákonarson

OS-89012/JHD-06 Mars 1989

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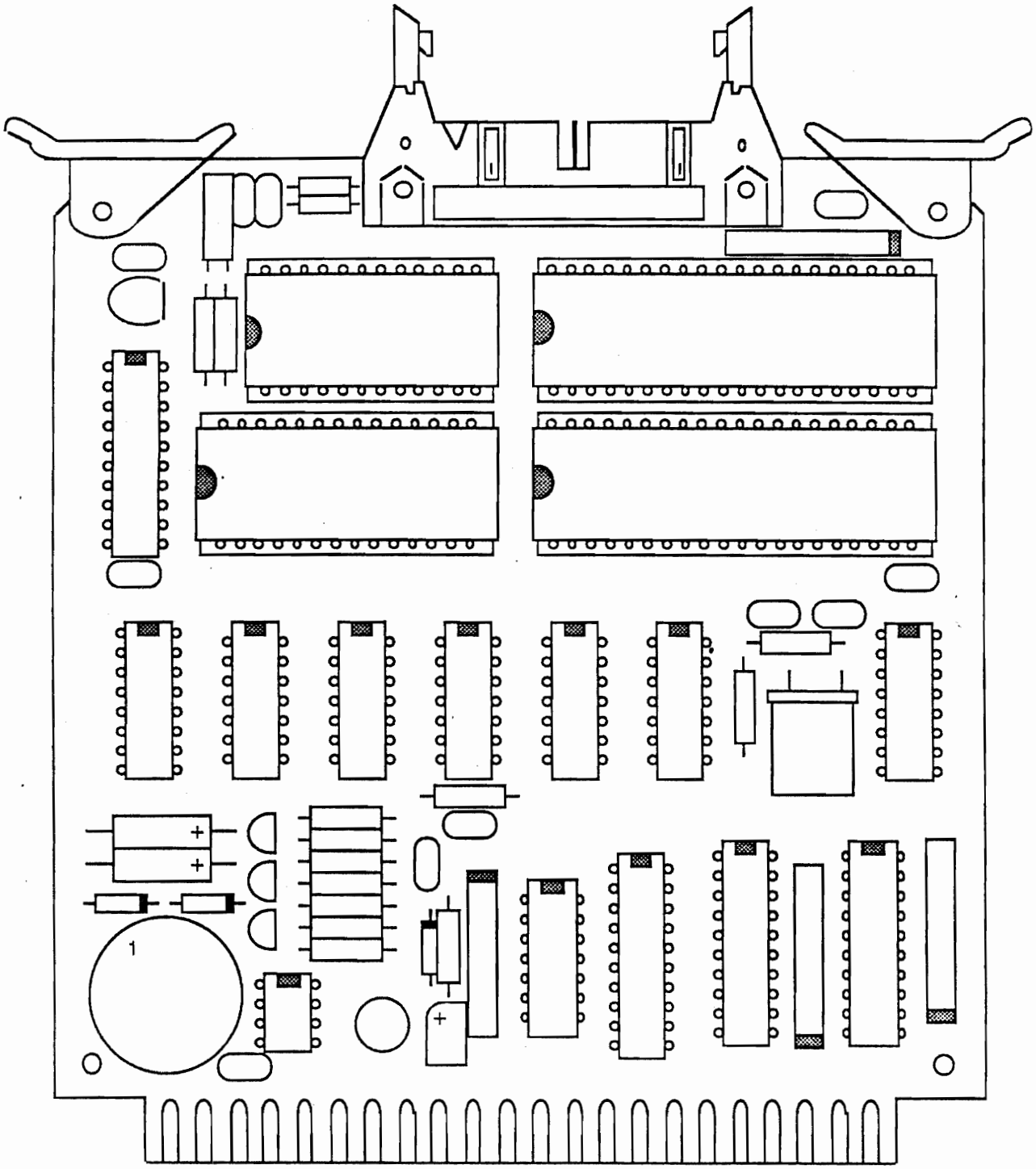
SKRÁ YFIR VIÐAUKA

VIÐAUKI D

Örtölvubretti

The CPU-801 MANUAL



Onset Computer Corporation
N. Falmouth, MA 02556

June 1986

CPU-801: CMOS Single Board Computer

Features

* 3 MHz NSC-800 CPU
* 178 bytes of onboard RAM
* 6K EPROM (27C64)
* 22 I/O Lines
* Two 16-bit timers
* Real-time clock
* Switching voltage regulator
* <5 milliwatt HYBERNATE™ mode
* <100 milliwatt WAIT mode
* five interrupts
* Power-on reset
* Power-on jump

Introduction

The CPU-801 has an NSC-800 CPU which executes the Z-80 instruction set, 178 bytes of RAM, 22 lines of I/O, 6K of CMOS EPROM, a real-time clock and a voltage regulator. The onboard memory and I/O are mapped into the top 8K of memory with the EPROM enabled at power-up or reset to accommodate disk based systems. In systems where the onboard complement of memory is sufficient, the CPU-801 can be remapped to place the EPROM in the bottom of memory so that the interrupt vectors point to EPROM locations. Designed for applications requiring low power consumption, the CPU-801 is fully compatible with all C-44 bus expansion cards. In its low power HYBERNATE mode the NSC-800's oscillator input is disabled, reducing the board's power consumption to less than five milliwatts. While executing, the board is fast enough to handle disk transfers on a polled basis.

The NSC-800

The NSC-800 CPU used in the CPU-801 is a CMOS microcomputer capable of executing the familiar Z-80 instruction set. The NSC-800 uses the advanced multiplexed structure employed by many CMOS microprocessors. This multiplexed structure is preserved in the C-44 bus, allowing connection of the CPU-801 to peripheral chips also using this structure. The four independently maskable interrupts and one non-maskable interrupt of the NSC-800 permit rapid response to external inputs. Running at 3 MHz, the CPU-801 has a minimum instruction execution time of only 1.33 microseconds.

178 bytes of RAM

The board's RAM resides in the NSC-810 port chip and 146818 real-time clock. The NSC-810 has 128 bytes; the RTC has 50.

27C64 EPROM

The CPU-801 has a 27C64 EPROM for program storage. Only 6K of this EPROM is available for program; the other 2K of memory space is allocated to the NSC-810 port chip, the real-time clock, and entry points for the HYBERNATE and WAIT modes. The EPROM is addressed between E000H and F7FFH, and the CPU-801 has a special circuit that forces all memory accesses to the EPROM on power-up. This circuit is disabled when the EPROM is read from its normal address.

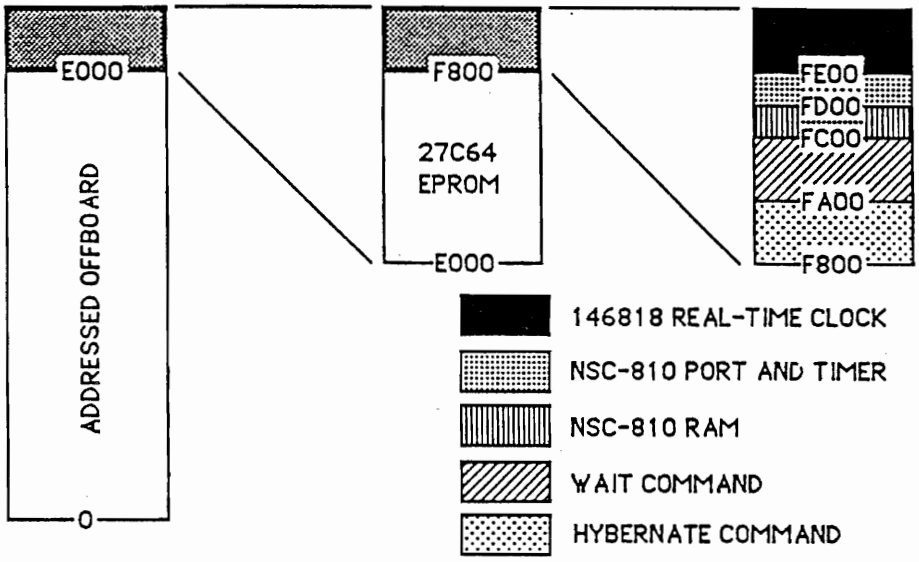
I/O Capabilities

The NSC-810 port chip provides the CPU-801 with 22 I/O lines which can be programmed to a wide variety of modes, including bit setting and clearing and strobed input and output. Two of the port lines can be programmed to make a 16 bit timer which can be used as either an event counter or signal generator. A second timer of the NSC-810 port chip (T0) has its input and output brought to the edge connector as well. By installing a jumper on the board the input to this timer can be tied to the system clock instead. The eight lines of one of the ports have one megohm pullups to facilitate connection to offboard switches.

The memory map

The CPU-801 can be configured two ways. In the default mode the onboard memory is mapped at the top of memory space, with the EPROM enabled at power-up or reset. When the board is used in an application not requiring additional memory, the board can be reconfigured to disable internal decoding of the top three address bits. This decodes all memory as onboard, placing the EPROM at the bottom of memory so that the vectored interrupts vector to EPROM locations.

The CPU-801 does not use any I/O space onboard, but appropriates the top 8K of address space for onboard use. This address space is partitioned as shown below. Note that this entire range (E000H-FFFFH) is reserved for onboard use, and cannot be addressed externally. All port space and all addresses below E000H are looked for offboard.



Address range	Usage
FE00H-FE3FH	146818 real-time clock
FD00H-FD19H	NSC-810 PORT and TIMER commands
FC00H-FC7FH	NSC-810 RAM
FA00H 512	WAIT mode command**
F800H 512	HYBERNATE command**
E000H-F7FFH = 1800h = 6144 byte	EPROM
0 - DFFFH	Addressed offboard*

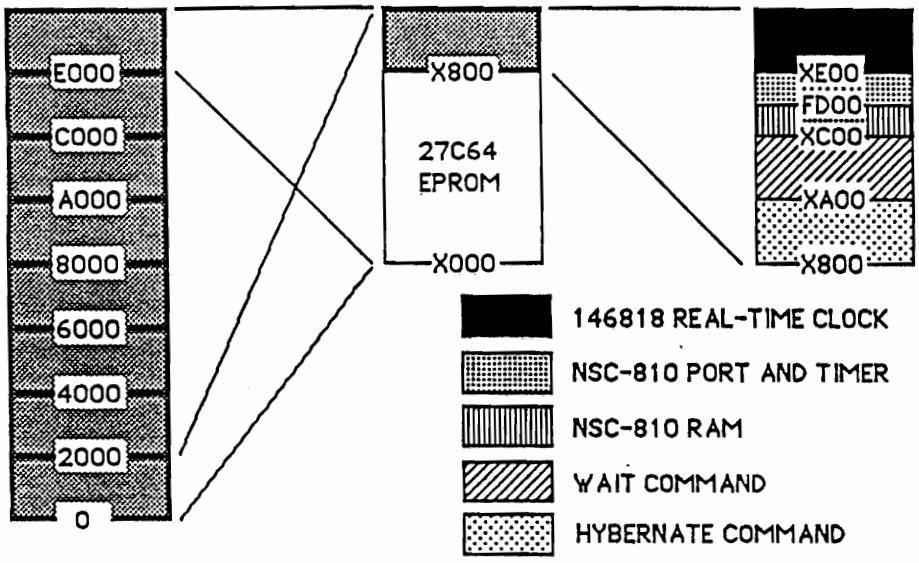
* On power-up or reset the EPROM will be enabled no matter what memory location is addressed until it is addressed at its normal memory location. See 'Power-on Jump' section on page 5.

** Writing to these locations causes the CPU-801 to drop into HYBERNATE or WAIT mode, from which it is awakened by either INT A, INT B, system reset, or asserting the WAKEUP line.

An alternate memory map

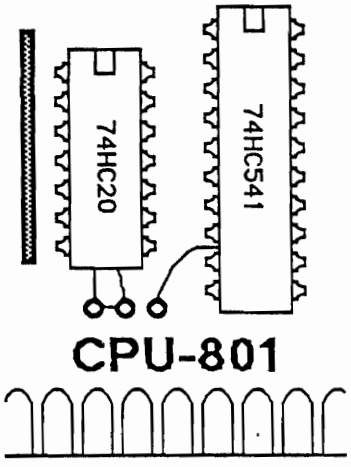
Not only is the restart location of the NSC-800 at zero, but all of the interrupts are vectored to addresses in the first page of memory. In applications where the CPU-801 is not used with an additional memory card, none of the interrupts can be used as they would be vectored to external addresses where there is no memory! To solve this problem the CPU-801 is equipped with an alternate memory addressing scheme.

By making one cut and jump you can reconfigure the board so that there is no external memory (port space is still referred offboard). The 8K block normally addressed onboard is mapped into all eight 8K blocks in the board's memory space. This places the EPROM in memory locations 0-17FF as well, so that the reset vectors can be in the EPROM.

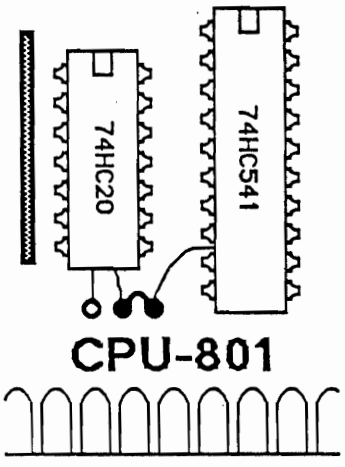


With this mapping the EPROM is addressed at location 0 so that the first instruction will disable the power-on jump, and you need not include the JMP E003 instruction used in the normal mapping.

To enable the alternate memory mapping, cut the trace between the two pads directly above the 'P' in 'CPU-801' located in the middle of the board near the edge connector fingers. Then jump the middle pad to the one to its right as shown in the figures below.



Standard memory map



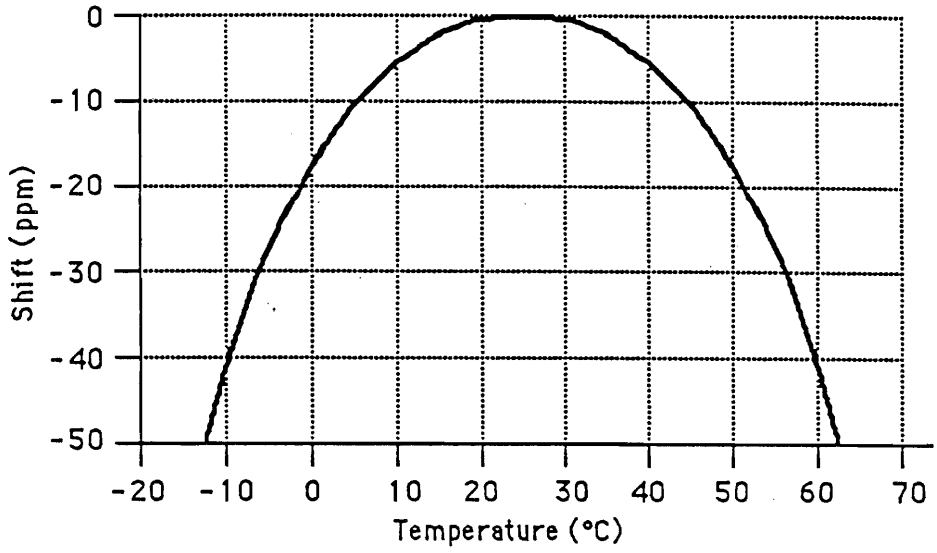
Alternate memory map

Power-on jump

The CPU-801 always addresses the lowest location of the EPROM on power-up by mapping the EPROM into all locations in address space 0-1FFF, 2000 - 3FFF etc. This is necessary since the power-on reset address of the NSC-800 is memory location 0, not in the EPROM, and for proper system operation the first instruction on power-up must be fetched from ROM. This unusual addressing mode will remain until the EPROM is addressed at its true location (E000). Accordingly the first instruction in the EPROM should be 'JMP 0E003'. This will disable the power-up addressing of the EPROM and start your program at E003.

Real-time clock

The 146818 real-time clock not only keeps track of time, but can also cause interrupts at specific times or at regular intervals. The RTC uses a 32.768 MHz crystal as its timebase. This crystal has a large temperature dependence as shown in the plot below.



The 146818 is multiply mapped in its address space, repeating every 64 locations from FE00 to FFC0. For simplicity we will refer to it only at its primary location FE00 to FE3F. Within this block, locations FE00 to FE0D are used by the clock for its time alarm and control registers. Locations FE0E through FE3F are usable as RAM. The CPU-801 monitor uses these locations for storage of its variables and stack. Details of the operation of the RTC are described in the accompanying 146818 manual.

The RTC's - IRQ output is connected to the INT A line (PIN F) so that sleep-wake control can be handled by this line. The RTC will only assert the interrupt line if its interrupt feature is enabled, so that INT A can be used for other purposes if desired.

Fully buffered bus

Thanks to the availability of fast CMOS buffer chips, it is possible to provide complete buffering of the lines coming from the CPU-801. This permits interfacing of the CPU-801 with the low power CMOS add-on boards of the C-44 bus. With full buffering, systems requiring ten or more boards can be designed without excessive timing skew.

Five interrupts

The CPU-801 has five interrupts: a non-maskable interrupt (NMI), and four independently maskable interrupts. Two of the maskable interrupts (INT A and INT B) awaken the CPU-801 from its HYBERNATE mode. The interrupts call specific locations in memory (the onboard EPROM). The call locations are shown in the table below.

C-44 bus	NSC-800	Call address	Pin Number
NMI	NMI	66H	9
INT A	RST A	3CH	F
INT B	RST B	34H	E
INT C	RST C	2CH	5
INT D *	INTR	38H	3

* Note that the IM 1 instruction (0EDH,56H) must be executed before INT D will work properly. This instruction places the NSC-800 in interrupt mode 1 which responds to an INTR with a call to location 38H.

HYBERNATE mode

Writing to memory location F800H puts the CPU-801 into its low-power HYBERNATE mode which stops the CPU's crystal and reduces the system supply voltage. The CPU stops in the middle of the write cycle of the instruction writing location F800H. At the same time the programmable voltage regulator reduces the supply voltage of the system to about 2.8 volts. In this state the current drain of the board is reduced to about 0.3 mA. Wake-up from the HYBERNATE mode can be initiated by a system reset, an interrupt A, an interrupt B, or a pulse on the WAKEUP line; any of these will cause the supply voltage to return to 5.0 volts. Instruction execution is resumed after the crystal oscillator has recovered (about a one millisecond delay). The CLOCK line is not driven while the board is in HYBERNATE mode.

WAIT mode

Writing to memory location FA00H puts the CPU-801 in a low-power WAIT mode in which the oscillator is kept running and the system supply voltage is not reduced, but program execution is halted. Recovery is made in the same manner as recovery from the HYBERNATE mode, except that no delay is involved.

Power consumption

The power consumption of the CPU-801 is a strong function of the operating mode, as shown in the table below. The current drain in HYBERNATE mode is independent of the memory segment from which it is entered. Note that in all cases below, the current drains are shown for the CPU-801 alone, with no external boards connected to it.

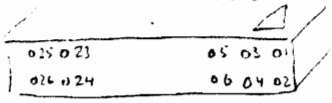
Vbat (volts)	27C64 EPROM (mA)	WAIT (mA)	HYBERNATE (mA)
6.5	24	13	0.5
8	21	12	0.4
10	18	11	0.3
12	16	9	0.3
15	14	7	0.25
18	12	6	0.25

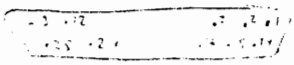
HYBERNATE-WAKE voltage cycle

The rise and fall times of the supply voltage of the CPU-801 are strongly dependent upon the capacitance of the system and the system current drain. When the CPU-801 is used by itself (offboard capacitance and current drain are negligible), the rise time and fall time of the supply are as follows:

Fall time	40 milliseconds
Rise time	300 to 100 microseconds (6.5 v to 18 BATTERY input)

This is of some importance, as the current drain of the system is a strong function of supply voltage, and accordingly remains high (>2 mA) as the system voltage drops to its 2.8 volt value during HYBERNATE mode. In calculating the average current drain for a system operating in HYBERNATE-WAKE cycles, the higher drain while supply voltage is falling must not be overlooked.





NSC-810A port pinout

Port A of the NSC-810A has 1 megohm pullup resistors to facilitate connection to switches. The pinout of the 26 pin ribbon cable connector is shown in the table below. The pin numbering on the connector corresponds to the wire number of the ribbon cable connector. Wire 26 of the ribbon cable is connected to the T0 output, and pin 2 to its input. Pin 3 of the connector is tied to the regulated supply voltage, and pin 1 is connected to ground.

DPIN = pinout; 25 pin D series is flat flathapial

Port A	Pin	D PIN	Port B	Pin	D PIN	PortC	Pin	D PIN
A7	10	18	B7	11	6			
A6	12	19	B6	13	7			
A5	14	20	B5	15	8	C5	8	17
A4	16	21	B4	17	9	C4	6	16
A3	18	22	B3	19	10	C3	4	15
A2	20	23	B2	21	11	C2	5	3
A1	22	24	B1	23	12	C1	7	4
A0	24	25	B0	25	13	C0	9	5
T0out	26	NC						
T0in	2	14						
GND	1	1						
Vreg	3	2						

Card edge connections

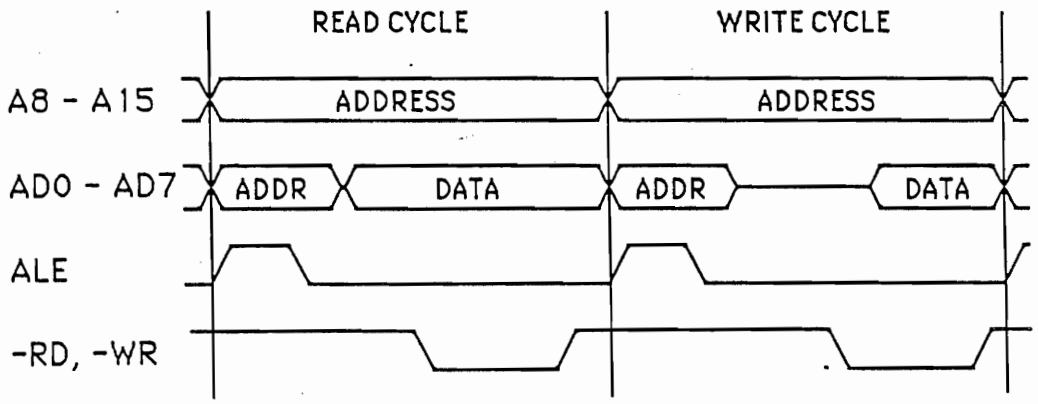
The definitions of the pins used by the CPU-801 are shown below. A minus sign preceding a signal indicates that its active level is negative. N.C. stands for no connection.

(Component side)		(Solder side)	
(1)	GROUND	(A)	GROUND
(2)	BATTERY	(B)	BATTERY
(3)	- INT D	(C)	- EXT RESET
(4)	N.C.	(D)	- RESET OUT
(5)	- INT C	(E)	- INT B
(6)	-WAKEUP	(F)	- INT A
(7)	N.C.	(H)	A13
(8)	N.C.	(J)	A12
(9)	- NMI	(K)	A11
(10)	CLOCK	(L)	A10
(11)	N.C.	(M)	A9
(12)	N.C.	(N)	A8
(13)	N.C.	(P)	AD7
(14)	N.C.	(R)	AD6
(15)	- READ	(S)	AD5
(16)	- WRITE	(T)	AD4
(17)	ALE	(U)	AD3
(18)	IO/-M	(V)	AD2
(19)	A15	(W)	AD1
(20)	A14	(X)	AD0
(21)	GROUND	(Y)	GROUND
(22)	Vreg	(Z)	Vreg

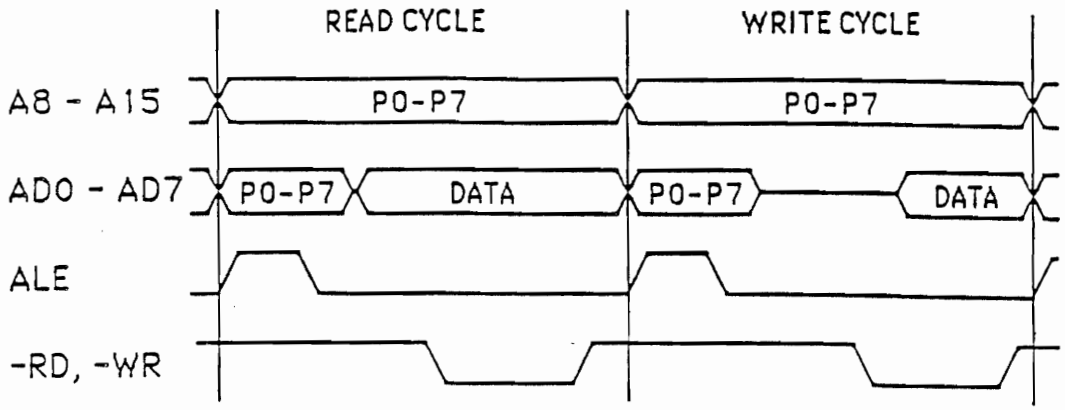
Edge connector pin definitions

Data and address bus

To minimize the number of lines needed to carry address and data, the C-44 bus multiplexes address and data. The upper eight address lines (A8-A15) carry memory and port addresses only, while the lower eight address lines (AD0- AD7) handle the data transfer as well. In a typical cycle A8-A15 will carry address information throughout, but AD0-AD7 will carry addresses only for the first part of the cycle, carrying data for the remainder of the cycle as shown below.



Similarly during a PORT cycle the port address is multiplexed with the data on the lines AD0 - AD7. Only eight bits are needed to specify a port address, and these eight bits are presented on both the upper and lower address lines as shown in the figure below.



This particular bus has two especially nice features. The first is that the multiplexed nature of the lower eight lines means that there are fewer lines on the bus, and correspondingly fewer lines on each board. This makes board layout easier, and also allows higher chip densities.

The other important feature is that the port address is carried on both AD0-AD7 and A8-A15. There are several port chips that expect the port address to be multiplexed onto the lower eight bits of the address lines, and these chips are particularly easy to connect to the C-44 bus. Having the port address available on both the upper and lower halves of the address bus makes decoding the port address for normal port chips easy as well. If a board has both ports and memory, one decode circuit can be used to decode both the port and the memory addresses.

Control lines

There are four important control lines on the C-44 bus: ALE, IO/-M, -RD, and -WR. These lines control the data flow on the bus and are described briefly below. Negatively asserted lines are indicated by a minus sign.

ALE — The falling edge of this line is used to latch the address from the AD0-AD7 lines for memory boards. Many port boards use the AD lines for data transfer only, and therefore can ignore this line.

-RD — When -RD is low, the CPU is expecting data from a peripheral. This line can be used to control the output direction of bidirectional buffers used to buffer the data from a peripheral board, as the CPU actually reads the bus one half cycle before the end of the -RD pulse.

-WR — When -WR is low, the AD lines contain data that is to be written to a memory or a port.

IO/-M — This line is high when the address lines are addressing port space, and low when they are addressing memory space. This line is a vital part of any decode circuit, and like the upper address lines, is valid long before the appearance of -RD or -WR.

Other lines of lesser importance

-RESET IN — This active low line is normally an input to the CPU only, and is used to perform a total system reset. The CPU-801 board has a power-on reset, but if an additional external reset is required, it should be tied to this line.

-RESET OUT — When this line is active (low), the CPU is being reset. Boards that need to be reset at power-on should use this line for that purpose.

CLOCK — This line provides a high frequency clock (1.5 MHz) to peripherals.

-INT A,B,C,D — When these interrupt lines are pulled to their active levels, the CPU performs a restart to a specific location in memory. These lines are all active low. These lines are pulled high on the CPU-801 by 4.7K resistors.

-WAKEUP — Asserting this line causes the CPU to exit either of its low power modes. The CPU will continue executing from the location where stopped.

-NMI — -NMI is a non-maskable interrupt. Like the INT A - INT D, this line forces the CPU-801 to restart to a specific memory location. This interrupt is not maskable, however, and therefore should be used with care, as it might interrupt the CPU during a critical operation. This interrupt is edge triggered and accordingly should be de-bounced.

Power lines

As the CPU-801 normally will run from batteries, it comes with an onboard regulator. This regulator runs from the H.C. BATTERY line and the regulated output is available at the Vreg output.

BATTERY — This is the input to the onboard regulator and can range from +6.5 to +18 volts without affecting the board's operation.

+5 — Regulated output from the CPU-801; +5 volts at all times except while in HYBERNATE mode when it is nominally 2.8 volts.

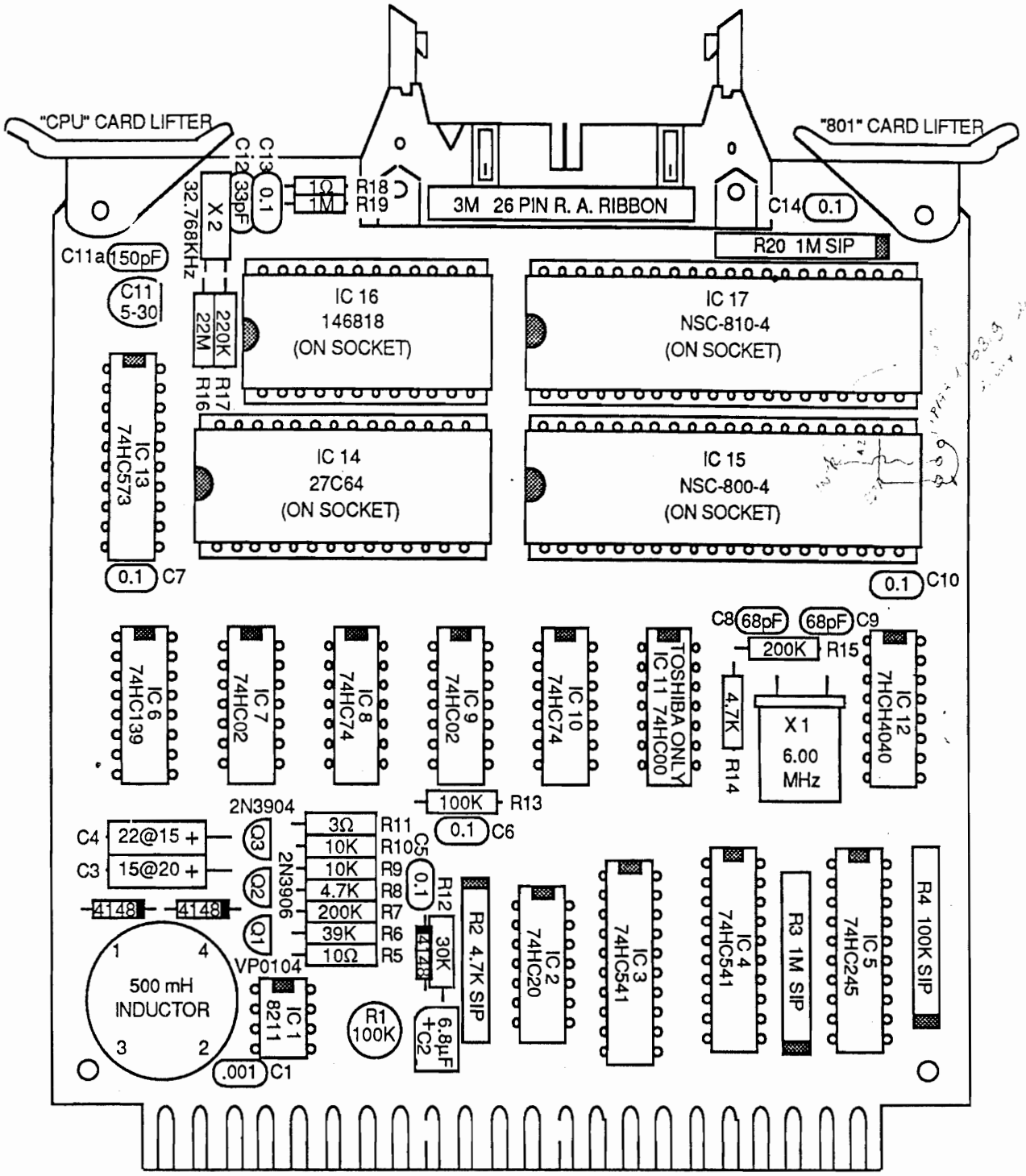
GROUND — Common return line for BATTERY and +5.

Calibration

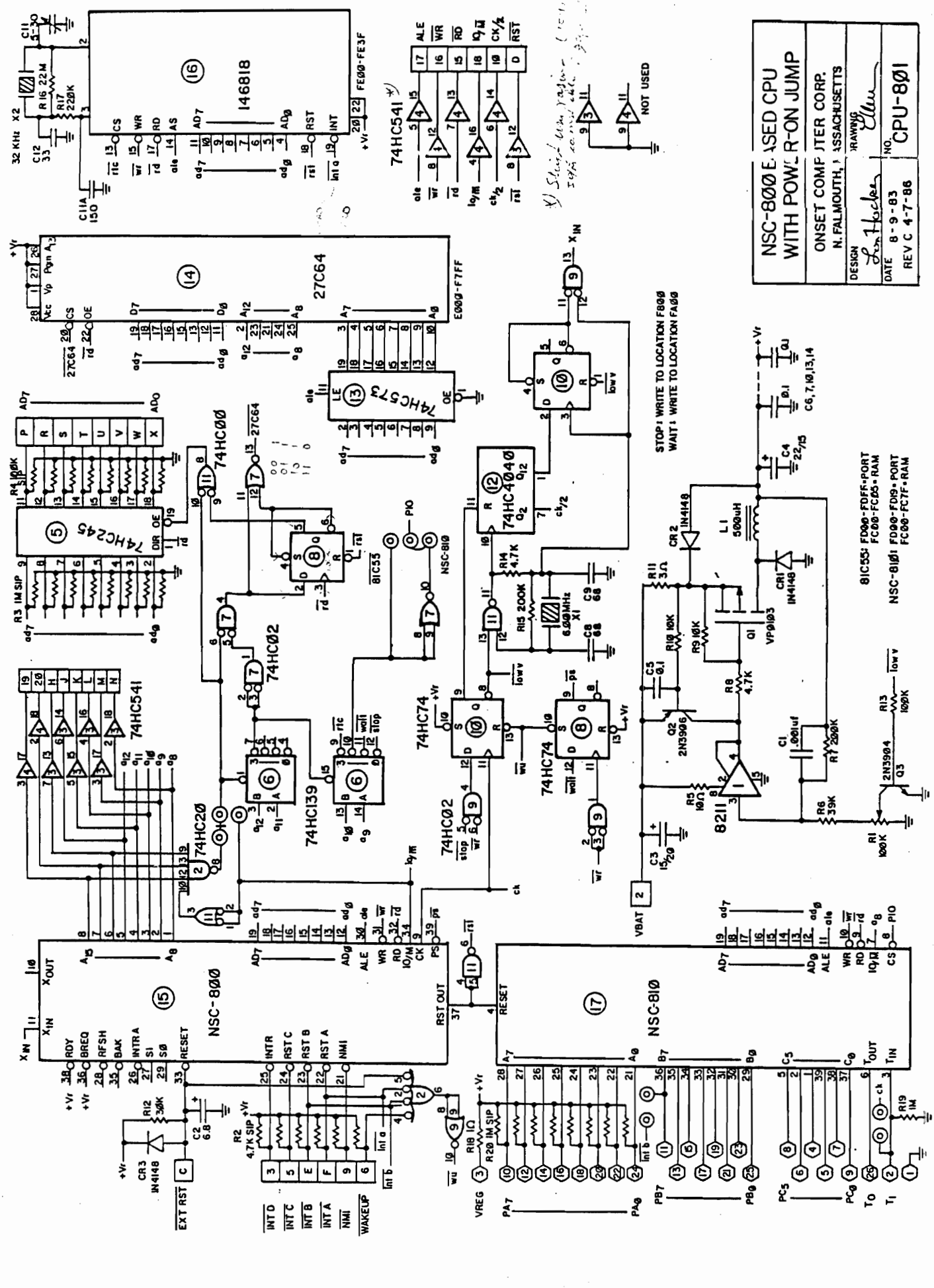
The CPU-801 has two adjustments: one sets the Vreg voltage, and another sets the real-time clock's timebase.

Vreg — The five volt supply for the board is set by a variable resistor just to the right of IC-1, the 8211 voltage regulator. We set Vreg to 5.00 volts with a BATTERY supply of 12 volts and with the CPU-801 running its monitor program, waiting for a keystroke.

RTC timebase — The 146818 real-time clock runs from a 32.768 KHz crystal. The frequency of this clock is set by adjusting the variable capacitor near the 146818. The CPU-801 monitor program sets the square wave output (pin 23) of the 146818 to 8 Hz. To set the crystal frequency adjust the variable capacitor until the period of the output at pin 23 is 0.1250000 sec.



Parts location drawing for CPU-801 rev B and C.


NSC-800 BASED CPU
WITH POWER-ON JUMP
ONSET COMPUTER CORP.
N. FALMOUTH, MASSACHUSETTS
DESIGN
DRAWING
DATE 8-9-83
REV C 4-7-86
NO. CPU-801
NOT USED
STOP: WRITE TO LOCATION F800
WAIT: WRITE TO LOCATION FA00
8155: FD00-FDFF=PORT FC00-FC05=RAM
NSC-810: FD00-FD19=PORT FC00-FC7F=RAM
NSC-800
NSC-810
8211
74HC541
74HC20
74HC02
74HC139
74HC74
74HC00
74HC245
74HC573
74HC4040
27C64
146818
EXT RST
WAKEUP
INT D
INT C
INT B
INT A
NMI

Before initializing the internal registers, the SET bit in Register B should be set to a "1" to prevent time/calendar updates from occurring. The program initializes the 10 locations in the selected format (binary or BCD), then indicates the format in the data mode (DM) bit of Register B. All 10 time, calendar, and alarm bytes must use the same data mode, either binary or BCD. The SET bit may now be cleared to allow updates. Once initialized the real-time clock makes all updates in the selected data mode. The data mode cannot be changed without reinitializing the 10 data bytes.

Table 3 shows the binary and BCD formats of the 10 time, calendar, and alarm locations. The 24/12 bit in Register B establishes whether the hour locations represent 1-to-12 or 0-to-23. The 24/12 bit cannot be changed without reinitializing the hour locations. When the 12-hour format is selected the high-order bit of the hours byte represents PM when it is a "1".

The time, calendar, and alarm bytes are not always accessable by the processor program. Once-per-second the 10 bytes are switched to the update logic to be advanced by one second and to check for an alarm condition. If any of the 10 bytes are read at this time, the data outputs are undefined. The update lockout time is 248 μs at the 4.194304 MHz and 1.048567 MHz time bases and 1948 μs for the 32.768 kHz time base. The Update Cycle section shows how to accommodate the update cycle in the processor program.

FIGURE 15 — ADDRESS MAP

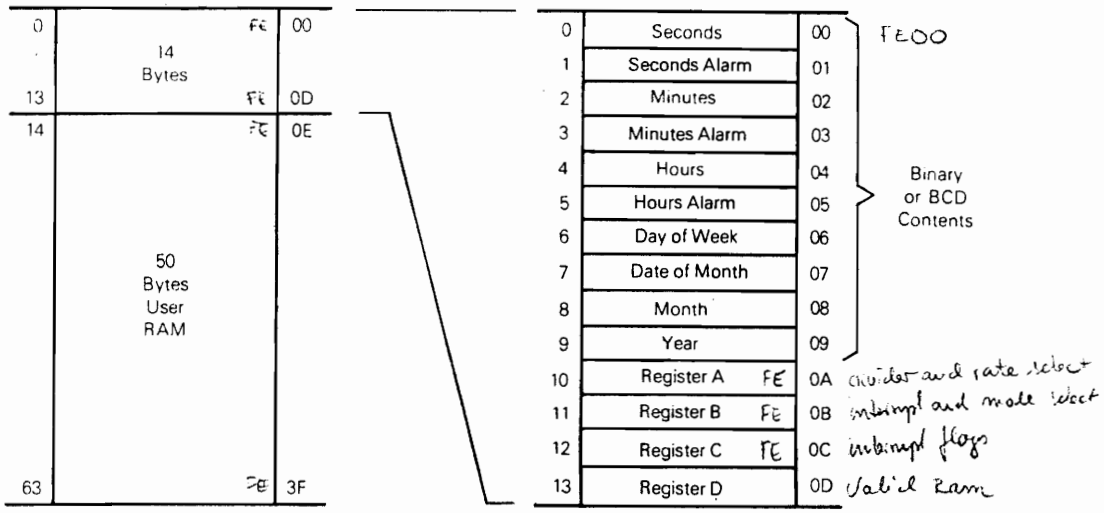


TABLE 3 — TIME, CALENDAR, AND ALARM DATA MODES

Address Location	Function	Decimal Range	Range		Example*	
			Binary Data Mode	BCD Data Mode	Binary Data Mode	BCD Data Mode
0	Seconds	0-59	$00-$3B	$00-$59	15	21
1	Seconds Alarm	0-59	$00-$3B	$00-$59	15	21
2	Minutes	0-59	$00-$3B	$00-$59	3A	58
3	Minutes Alarm	0-59	$00-$3B	$00-$59	3A	58
4	Hours (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours (24 Hour Mode)	0-23	$00-$17	$00-$23	05	05
5	Hours Alarm (12 Hour Mode)	1-12	$01-$0C (AM) and $81-$8C (PM)	$01-$12 (AM) and $81-$92 (PM)	05	05
	Hours Alarm (24 Hour Mode)	0-23	$00-$17	$00-23	05	05
6	Day of the Week Sunday = 1	1-7	$01-$07	$01-$07	05	05
7	Date of the Month	1-31	$01-$1F	$01-$31	0F	15
8	Month	1-12	$01-$0C	$01-$12	02	02
9	Year	0-99	$00-$63	$00-$99	4F	79

*Example: 5:58:21 Thursday 15 February 1979 (time is AM)

NSC810A Functional Description (Continued)

I/O PORTS

There are three I/O ports (labeled A, B and C) on the NSC810A. Ports A and B are 8-bits wide; port C is 6-bits wide. These ports transfer data between the CPU bus and the peripheral bus and vice versa. The way in which these transfers are handled depends upon the currently programmed operating mode.

The NSC810A can be programmed to operate in four different modes. One of these modes (Basic I/O) allows direct transfer of I/O data without any handshaking between the *NSC810A and the peripheral*. The other three modes (Strobed I/O) provide for timed transfers of I/O data with handshaking between the NSC810A and the peripheral.

Determination of the NSC810A port's mode, data direction and data is done by five registers which are under program control. The Mode Definition Register determines in which of the four I/O modes the chip will operate. Another register (Data Direction Register) establishes the data direction for each bit in that port. The Data Register holds data to be transferred or that which was received. The final two registers per port allow individual data register bits to be cleared (Bit-Clear Register) or data register bits to be set (Bit-Set Register).

Operation during Strobed I/O utilizes two of the port C pins for handshaking and one port C pin to interrupt the CPU.

Registers

As indicated in the overview, programmable registers control the flow of data through the ports. Table I shows the registers of the NSC810A. All registers affecting I/O transfers are in the first grouping of this table.

• Mode Definition Register (MDR)

The MDR determines the operating mode for port A and whether or not the lower 3-bits of port C will be used for handshaking (Strobed I/O). Port B always transfers data via the Basic I/O mode, regardless of how the MDR is programmed. The upper 3-bits of port C will transfer data via the Basic I/O mode even when the lower 3-bits are programmed for handshaking (Strobed I/O).

The four modes are as follows:

Mode 0—Basic I/O (Input or Output)

Mode 1—Strobed Mode Input

Mode 2—Strobed Mode Output (Active Peripheral Bus)

Mode 3—Strobed Mode Output (TRI-STATE Peripheral Bus)

The address assignment of the MDR is xxx00111 as shown in Table I. The upper 3 "don't care" bits are determined by the users decode logic (chip enable address). Table II specifies the data that must be loaded into the MDR to select the mode.

• Data Direction Registers (DDR)

Each port has a DDR that determines whether an individual port bit will be an input or an output. If DDR for the port bit is set to a 1, then that port bit is an output. If its DDR is reset to a 0, then it is an input. The DDR bits cannot be individually written to; the entire DDR register is affected by a write to the DDR. Thus, all data bits written must be consistent for all desired port bit directions.

TABLE I. I/O and Timer Address Designations

8-Bit Address Field Bits								Designation I/O Port, Timer, etc.	R (Read) W (Write)
7	6	5	4	3	2	1	0		
x	x	x	0	0	0	0	0	Port A (Data)	R/W
x	x	x	0	0	0	0	1	Port B (Data)	R/W
x	x	x	0	0	0	1	0	Port C (Data)	R/W
x	x	x	0	0	0	1	1	Not Used	**
x	x	x	0	0	1	0	0	DDR - Port A	W
x	x	x	0	0	1	0	1	DDR - Port B	W
x	x	x	0	0	1	1	0	DDR - Port C	W
x	x	x	0	0	1	1	1	Mode Definition Reg.	W
x	x	x	0	1	0	0	0	Port A - Bit-Clear	W
x	x	x	0	1	0	0	1	Port B - Bit-Clear	W
x	x	x	0	1	0	1	0	Port C - Bit-Clear	W
x	x	x	0	1	0	1	1	Not Used	**
x	x	x	0	1	1	0	0	Port A - Bit-Set	W
x	x	x	0	1	1	0	1	Port B - Bit-Set	W
x	x	x	0	1	1	1	0	Port C - Bit-Set	W
x	x	x	0	1	1	1	1	Not Used	**
x	x	x	1	0	0	0	0	Timer 0 (LB)	*
x	x	x	1	0	0	0	1	Timer 0 (HB)	*
x	x	x	1	0	0	1	0	Timer 1 (LB)	*
x	x	x	1	0	0	1	1	Timer 1 (HB)	*
x	x	x	1	0	1	0	0	STOP Timer 0	W
x	x	x	1	0	1	0	1	START Timer 0	W
x	x	x	1	0	1	1	0	STOP Timer 1	W
x	x	x	1	0	1	1	1	START Timer 1	W
x	x	x	1	1	0	0	0	Timer 0 Mode	R/W
x	x	x	1	1	0	0	1	Timer 1 Mode	R/W
x	x	x	1	1	0	1	0	Not Used	**
x	x	x	1	1	0	1	1	Not Used	**
x	x	x	1	1	1	0	0	Not Used	**
x	x	x	1	1	1	0	1	Not Used	**
x	x	x	1	1	1	1	0	Not Used	**
x	x	x	1	1	1	1	1	Not Used	**

x = don't care

LB = low-order byte

HB = high-order byte

* A write accesses the modulus register, a read the read buffer.

** A read from an unused location reads invalid data, a write does not affect any operation of NSC810A.

TABLE II. Mode Definition Register Bit Assignments

Mode	Bit 7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	0
1	x	x	x	x	x	x	0	1
2	x	x	x	x	x	0	1	1
3	x	x	x	x	x	1	1	1

31/3/87

ONSET COMPUTER CORP. TEST

CPU-801 TEST S.N. 558

BURN-IN 90 HOURS AT 70 DEG C

MIN EXECUTION VOLT <2.8

VOLTAGES	6.5 V supply	12 V supply	18V supply
Vreg	4.89	5.00	5.09
Vhyb	2.75	2.77	2.77

SYSTEM CLOCK FREQUENCY 1.500222

RTC PERIOD .125000 RTC SET AND CHECK ✓

CURRENT DRAIN (mA)

	6.5 V supply	12 V supply	18 V supply
XEQ (EPROM)	22.3	13.4	9.7
HYBERNATE	.089	.056	.047
WAIT	9.3	5.7	4.0

MEM TEST (FC00-FC7F) ✓

OFFBOARD TESTS: MEMORY TEST ✓ PORT TEST ✓

INTERRUPTS INT A ~~INT B~~ ✓ INT C ✓ INT N ✓ WAKE UP ✓

COMMENTS: _____

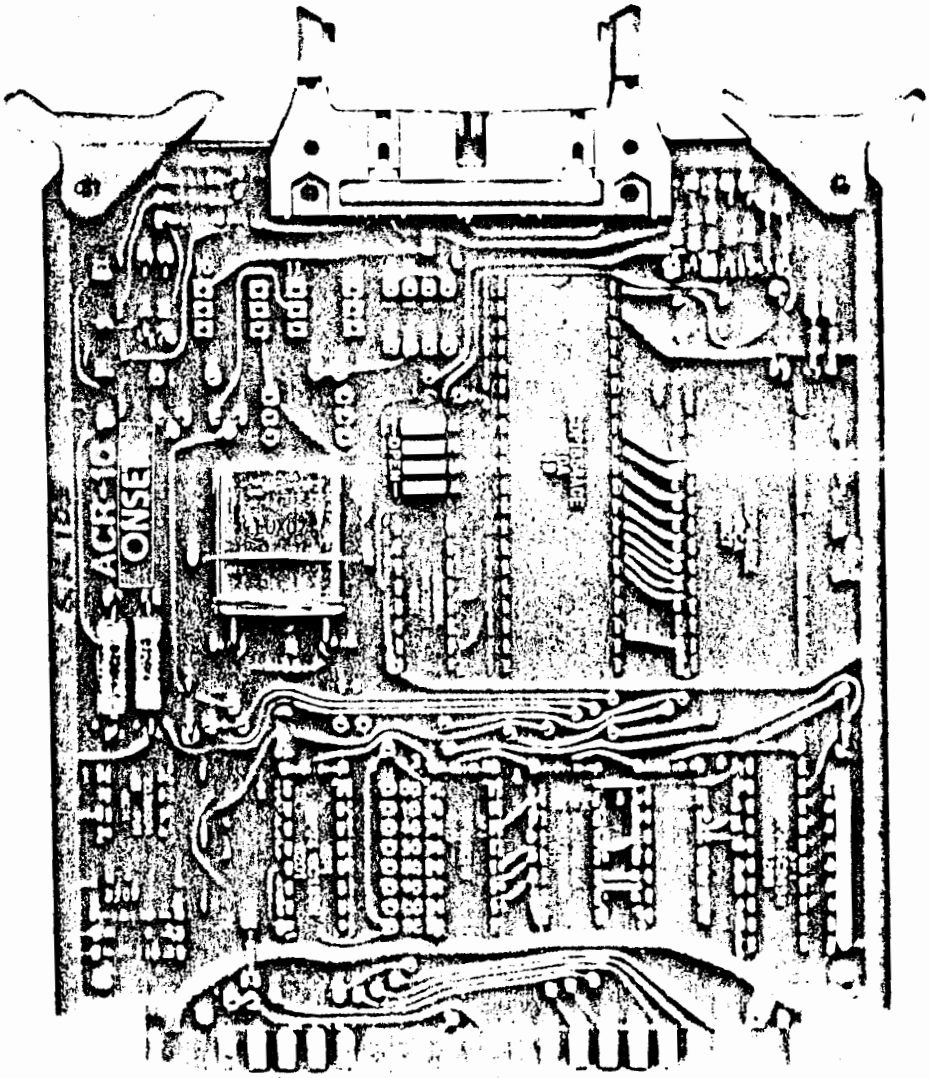
ASM C/R INSP. BY BCG TESTED BY [illegible] DATE 11-6-86

ONSET COMPUTER CORP.

VIÐAUKI E

Samskiptabretti

The ACR-10 Manual



ONSET
Computer Corp.
199 Main St.
P.O. Box 1016
N. Falmouth, MA 02556

February 1983

ACR-10

CMOS UART AND MATH BOARD

FEATURES:

* RS-232 INTERFACE
* 14 BAUD RATES; 50 TO 19200 BAUD
* +/- 7 VOLT OUTPUT LEVELS
* 1855 MULTIPLY/DIVIDE CHIP
* FULLY BUFFERED INTERFACE
* JUMPER ADDRESSABLE TO ANY OF 8 LOCATIONS
* <30 MICROAMP DRAIN TOTAL POWER DOWN MODE
* C-44 BUS COMPATIBILITY

INTRODUCTION

The ACR-10 is a combination UART and MULTIPLY/DIVIDE board for the C-44 bus. All standard baud rates from 50 to 19200 baud can be selected by the DIP switch on the board. The 1855 provides either an 8-bit X 8-bit multiply or a 16-bit/8-bit divide in about 9 microseconds (not including setup). Either or both the UART and math chip can be disabled under software control, minimizing the board's power consumption. The board initializes to its powered-down state.

BOARD ADDRESS

The default address of the board is 0D0H - 0DFH, but it can be re-addressed to any of seven other memory locations: 0 - 0FH, 10H - 1FH, 40H - 4FH, 50H - 5FH, 80H - 8FH, 90H - 9FH, or 0C0H - 0CFH. The board is re-addressed by moving a jumper in the address definition area at the bottom of the board. In subsequent discussions of port addressing, the default board address of 0D0H - 0DFH will be assumed.

ONBOARD ADDRESS SPACE

The RCA protocol specifies a Read/-Write line and a data strobe (like the MOTOROLA protocol in that respect). In order to satisfy the setup time requirements of the 1854 and 1855 chips it was necessary to use an address line (A8) to specify whether a Read or a Write is taking place. As a result all reads from these chips occur at odd addresses, and all writes occur at even addresses.

ADDRESS	FUNCTION	
	READ	WRITE
D0-D3	-----	BIT 7=MATH ENABLE BIT 0=UART ENABLE
D4	-----	UART DATA
D5	UART DATA	-----
D6	-----	UART CONTROL
D7	UART STATUS	-----
D8	-----	1855 X-REGISTER
D9	1855 X-REGISTER	-----
DA	-----	1855 Z-REGISTER
DB	1855 Z-REGISTER	-----
DC	-----	1855 Y-REGISTER
DD	1855 Y-REGISTER	-----
DE	-----	1855 CONTROL
DF	1855 STATUS	-----

THE UART

The board uses the 1854 UART which provides programmable word length, parity and number of stop bits. The baud rate is selected by an external baud rate generator that can be switch selected to provide the rate outputs necessary to generate the baud rates of 50 to 19200 baud. The switch settings necessary to provide these rates are shown in the table below. An onboard regulator and voltage inverter generates the +8v, -7.5 v EIA levels from the battery supply input. The output level converters use VMOS transistors to provide high efficiency outputs pulling to the power supply rails.

BAUD RATE SWITCH

SWITCH 1	SWITCH 2	SWITCH 3	SWITCH 4	RATE
OPEN	OPEN	OPEN	OPEN	110
OPEN	OPEN	OPEN	CLOSED	150
OPEN	OPEN	CLOSED	OPEN	300
OPEN	OPEN	CLOSED	CLOSED	2400
OPEN	CLOSED	OPEN	OPEN	1200
OPEN	CLOSED	OPEN	CLOSED	1800
OPEN	CLOSED	CLOSED	OPEN	4800
OPEN	CLOSED	CLOSED	CLOSED	9600
CLOSED	OPEN	OPEN	OPEN	2400
CLOSED	OPEN	OPEN	CLOSED	600
CLOSED	OPEN	CLOSED	OPEN	200
CLOSED	OPEN	CLOSED	CLOSED	134.5
CLOSED	CLOSED	OPEN	OPEN	75
CLOSED	CLOSED	OPEN	CLOSED	50
CLOSED	CLOSED	CLOSED	OPEN	19200
CLOSED	CLOSED	CLOSED	CLOSED	19200

ENABLING THE UART

Bit 0 of port D0 controls the power to both the baud rate generator and the EIA level supplies. When a 0 is written to this bit, the supplies are cut; when 1 is written to this bit, the power is turned on. A reset pulse from the CPU board (on pin D of the edge connector) turns the supplies off. A wait of about 0.1 second is necessary before using the UART after powering it up to give the supplies time to stabilize, and let the baud rate generator stabilize.

When powered down the UART's output is near ground level, an indeterminate region for RS-232's EIA levels.

UART TEST PROGRAM

This test program simply echos incoming characters. The first test version is for the CPU-6805A. Load it starting at 400H in RAM using monitor's SUBSTITUTE command, and then jump to START using the GOTO command. Notice that this program does not look for the transmitter to be empty, and works only because the timing is established by the incoming data.

```
START:  LDA$ 01          ;A6 01      ENABLE UART
        STA0 D0          ;B7 D0
        LDA$ 18          ;A6 18      SET UP 8 DATA BITS,
        STA0 D6          ;B7 D6      1 STOP BIT, ODD PARITY

X:      LDA0 D7          ;B6 D7      WAIT FOR INCOMING CHARACTER
        AND$ 01          ;A4 01      (COULD HAVE USED BIT TEST &
        BEQ X            ;27 FA      JUMP TO SAVE CODE)

        LDA0 D5          ;B6 D5      THEN ECHO IT
        STA0 D4          ;B7 D4      BACK OUT UART
        JUMP START       ;CC 04 00   ;AND TRY AGAIN
```

CPU-800A or CPU-8085 fanciers can use this translation of the above code. Use the RAM starting at 1040H.

```
START:  MVI A,01         ;3E 01      ENABLE UART
        OUT D0           ;D3 D0
        MVI A,18         ;3E 18      8 CHARACTERS (= 18 for 8,1,N)
        OUT D6           ;D3 D6      1 STOP BIT, ODD PARITY

X:      IN D7            ;DB D7      WAIT FOR INCOMING CHARACTER
        ANI 01           ;E6 01
        JZ X             ;CA 48 10

        IN D5            ;DB D5      ECHO CHARACTER
        OUT D4           ;D3 D4      BACK OUT UART
        JMP START        ;C3 40 10   AND START AGAIN
```

Putc: PUSH AF
IN A,07
AND 20
JR Z,loop
POP AF
OUT (D4),A
RET

CONNECTING TO THE UART

The serial data connections to the UART are made to a 26-pin ribbon cable connector at the top of the board. The pinout of this connector was chosen so that a ribbon cable connection to a 25-pin D-Subminiature connector will bring the serial data and ground connections to the proper pins for a peripheral device. The ribbon cable connections are shown below. The wire number is the same as the pin number at the board.

PIN NUMBER AT BOARD	PIN NUMBER ON D-SUBMIN	FUNCTION
1	1	GROUND
3	2	UART OUTPUT
5	3	UART INPUT
13	7	GROUND
22	24	GROUND
23	25	GROUND
25	13	EXTERNAL STATUS BIT (INPUT)
26	---	PERIPHERAL STATUS INTERRUPT

These last four have nothing to do with the EIA interface, but can be used to announce the connection of an external device to the connector. The two status lines have pullups, and grounding them sets the flag in the UART.

POWER CONSUMPTION

The power consumption of the ACR-10 is a strong function of the operating mode. When a load is connected to the output of the UART the current drain reflects this (when UART is enabled). A 10K load increases the BATTERY LINE drain by about 1 mA from the typical values shown below.

STATE	MODE	Vbat LINE	Vreg LINE
BOTH DISABLED	ACTIVE	<0.01 mA	0.5 mA
BOTH DISABLED	STOP (HYB)	<0.01 mA	<0.01 mA
MATH ONLY	ACTIVE	<0.01 mA	0.7 mA
MATH ONLY	STOP (HYB)	<0.01 mA	0.02 mA
UART ONLY	ACTIVE	2.8 mA	2.5 mA
UART ONLY	STOP (HYB)	1.5 mA	1.2 mA
BOTH ENABLED	ACTIVE	2.8 mA	2.8 mA
BOTH ENABLED	STOP (HYB)	1.5 mA	1.2 mA

JUMPER OPTIONS

By adding a jumper, you can make the UART cause interrupts on a variety of status conditions. This pair of pads is located above and slightly to the right of IC-2. Connecting this pair of pads connects the interrupt output of the 1854 UART to the INT A line of the bus. This connection is recommended for the CPU-800A or CPU-8085 only, as the -INT output of the 1854 is always active and will conflict with that of the 6818 of the CPU-6805A.

The board has etches for a current loop interface instead of the RS-232 EIA levels. This interface is optional, but has the disadvantage that it cannot be disabled.

A FULLY BUFFERED BUS

Thanks to the recent introduction of TTL compatible CMOS buffer chips, it has been possible to provide complete buffering of the address, data and control lines coming from the ACR-10. This keeps the capacitive loading of the bus low, permitting at least 10 memory and/or port expansion boards per system without causing excessive skew.

THE HYBERNATE MODE

C-44 bus CPU cards have low power modes that reduce the Vreg supply voltage to about 3.0 volts. Since the ACR-10's 5 volt supply comes from this source, the board sees a reduced supply during the HYBERNATE states of these CPU's. This is not a problem for any of the parts on the board.

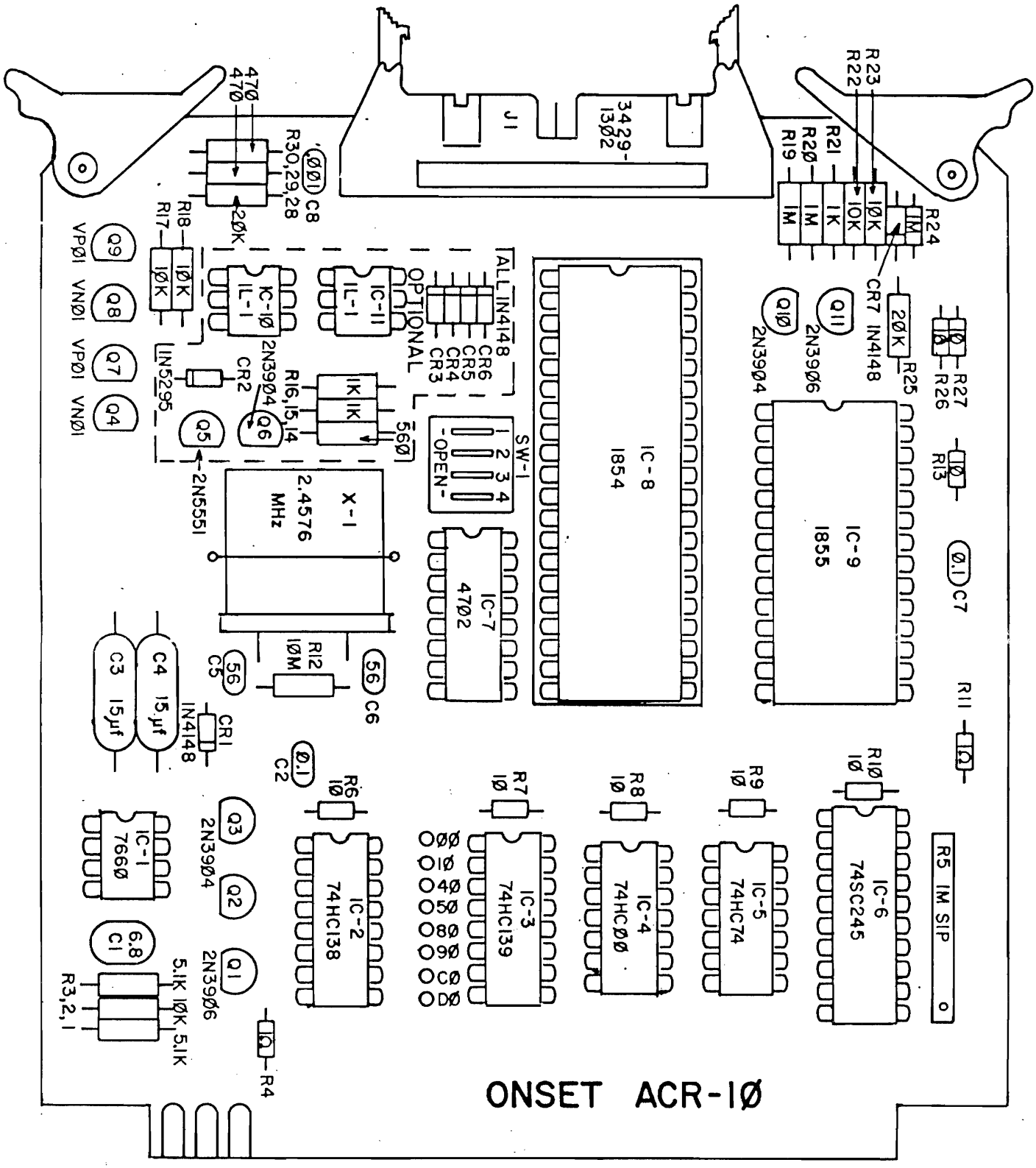
CHECKING THE CURRENT DRAIN

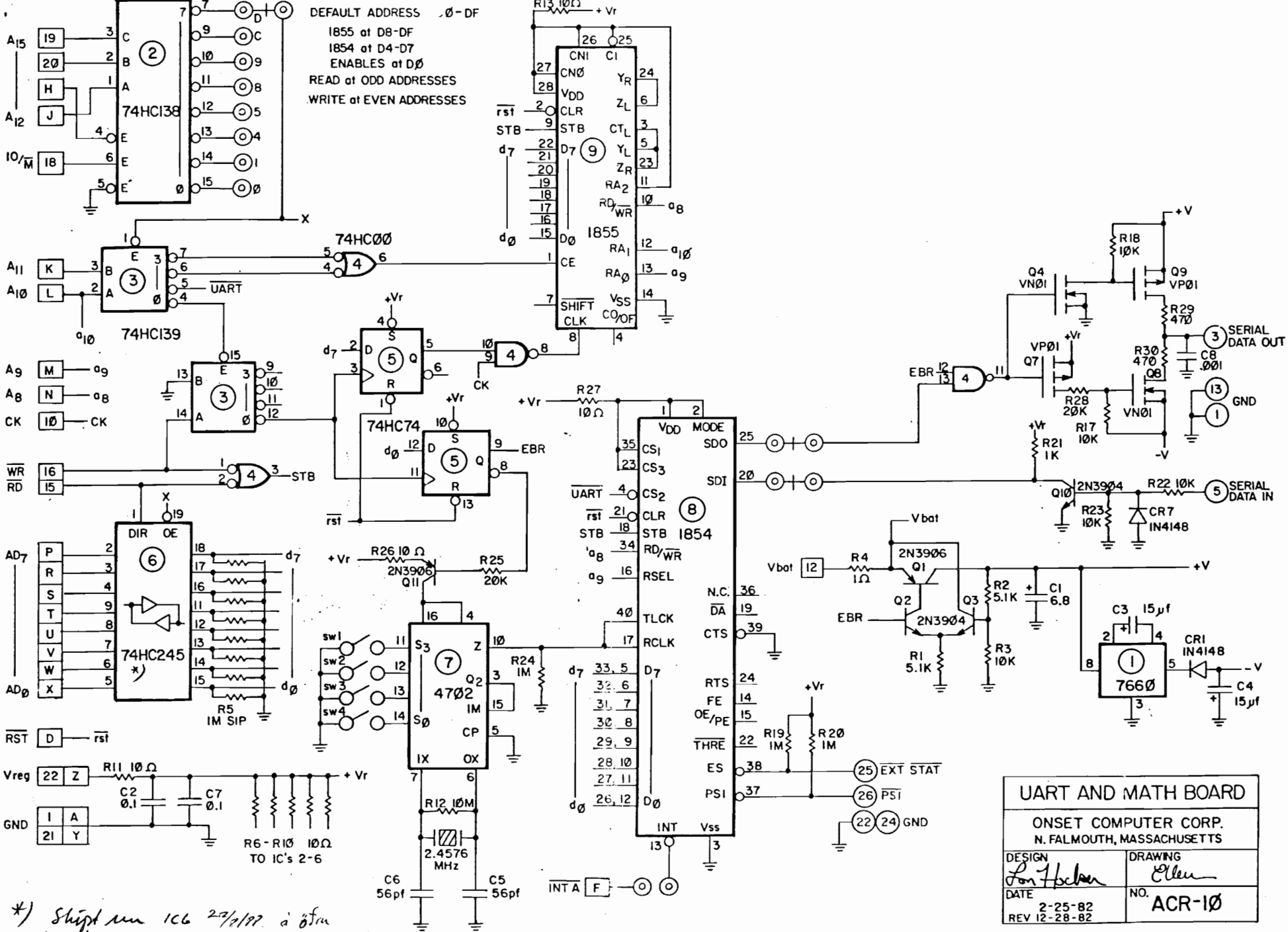
There are current sensing resistors for all IC's on the ACR-10. These resistors make it possible to measure the current usage of the IC's during checkout, and greatly simplify tracking down failures. Board current sense resistors allow monitoring current usage from both the regulated 5 volt supply and the battery supply.

CARD EDGE CONNECTION FOR THE ACR-10

The definition of the pins used by the ACR-10 are shown below; they are totally compatible with the C-44 bus. A minus sign preceding a signal indicates that its active level is negative. N.C. indicates that no connection is made to that line.

(COMPONENT SIDE)		(SOLDER SIDE)	
(1)	GROUND	(A)	GROUND
(2)	N.C.	(B)	N.C.
(3)	N.C.	(C)	N.C.
(4)	N.C.	(D)	-RESET OUT
(5)	N.C.	(E)	N.C.
(6)	N.C.	(F)	INT A
(7)	N.C.	(H)	A13
(8)	N.C.	(J)	A12
(9)	N.C.	(K)	A11
(10	CLOCK	(L)	A10
(11)	N.C.	(M)	A9
(12)	BATTERY	(N)	A8
(13)	N.C.	(P)	AD7
(14)	N.C.	(R)	AD6
(15)	- READ	(S)	AD5
(16)	- WRITE	(T)	AD4
(17)	N.C.	(U)	AD3
(18)	IO/-M	(V)	AD2
(19)	A15	(W)	AD1
(20)	A14	(X)	AD0
(21)	GROUND	(Y)	GROUND
(22)	Vreg	(Z)	Vreg

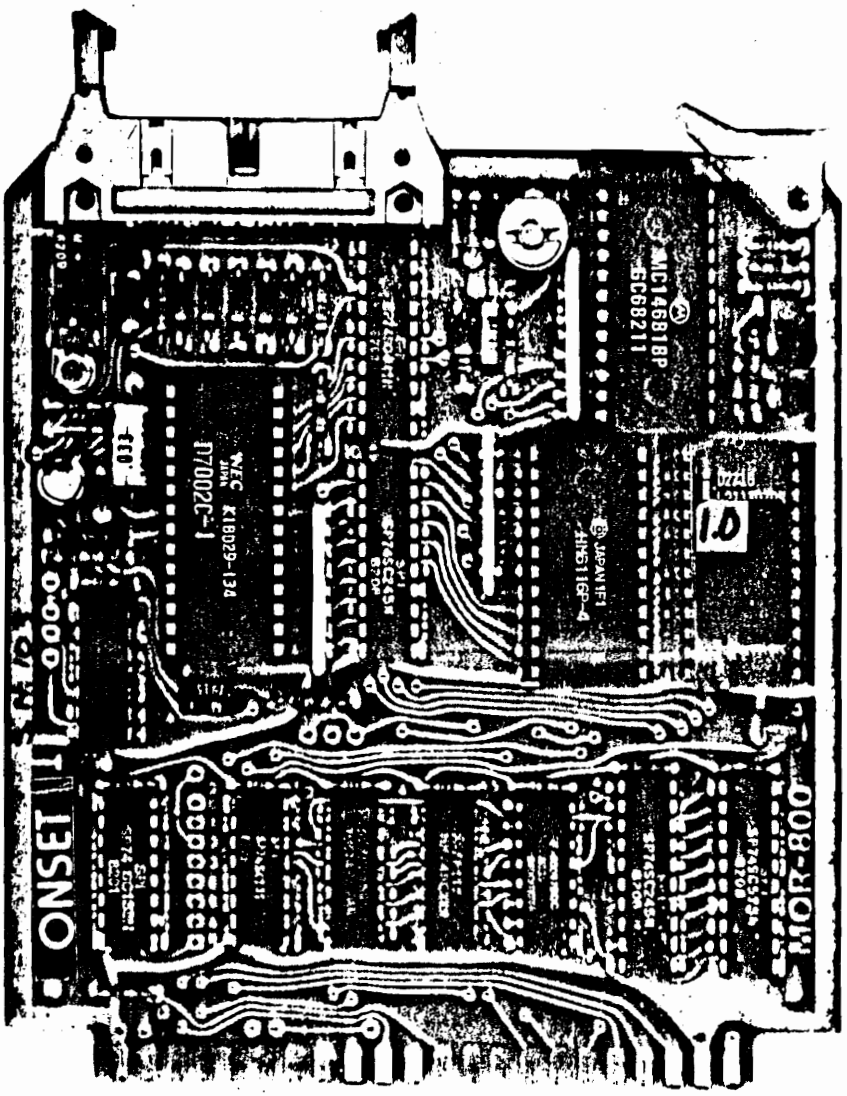

ONSET ACR-10
J1
3429-1302
IC-8 1854
IC-9 1855
IC-6 74SC245
IC-5 74HC74
IC-4 74HC00
IC-3 74HC139
IC-2 74HC138
IC-1 7660
IC-7 4702
IC-10
IC-11
X-1 2.4576 MHz
SW-1 OPEN
ALL IN4148
OPTIONAL
R5 1M SIP
R11 10
R24 1M
R23 10K
R22 10K
R21 1K
R20 1M
R19 1M
R25 20K
R26 10
R27 10
R13 10
R18 10K
R17 10K
R16,15,14 1K 1K
R12 10M
R10 10
R9 10
R8 10
R7 10
R6 10
R4 10
R3,2,1 5.1K 10K 5.1K
CR7 IN4148
CR6 CR5 CR4 CR3
CR2 IN5295
CR1 IN4148
Q10 2N3904
Q11 2N3906
Q9 VP01
Q8 VN01
Q7 VP01
Q4 VN01
Q6 2N3904
Q5 2N5551
Q3 2N3904
Q2
Q1 2N3906
C8 R30,29,28 470 470 20K
C7 .01
C6 56
C5 56
C4 15µf
C3 15µf
C2 .01
C1 6.8


DEFAULT ADDRESS ØØ-DF
1855 at D8-DF
1854 at D4-D7
ENABLES at DØ
READ at ODD ADDRESSES
WRITE at EVEN ADDRESSES
74HC138
74HC139
74HCØØ
74HC74
74HC245 *)
1855
1854
4702
7660
2N3904
2N3906
UART AND MATH BOARD
ONSET COMPUTER CORP.
N. FALMOUTH, MASSACHUSETTS
DESIGN Lon Hoban
DRAWING Ellen
DATE 2-25-82
REV 12-28-82
NO. ACR-ØØ
*) Skipt um ICs 27/2/82 á öfrum brettinum (24/1) EHH

VIÐAUKI F

A/D bretti

The MOR-800 Manual



ONSET
Computer Corp.
199 Main St.
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February 1983

10-BIT A TO D CONVERTER

FEATURES:

* 4-CHANNEL A TO D CONVERTER
* 10-BIT ACCURACY
* 11-BIT REPEATABILITY
* 12-BIT RESOLUTION
* 0-2.5 VOLT INPUT RANGE
* OPTIONAL REAL-TIME CLOCK
* 2K BYTE 6116 STATIC RAM
* 27C16 EPROM
* <30 MICROAMP DRAIN OFF-LINE

INTRODUCTION

The MOR-800 10-bit A to D converter card has a four-channel single-ended converter that accepts inputs covering the range of 0 to 2.5 volts. The converter can be completely powered down to give a quiescent current drain of less than 30 microamps for this section of the board. An optional 6818 real-time clock can be installed on the board to provide simplified time-keeping for CPU-800A and CPU-8085 based systems (CPU-6805A based systems already have an RTC). A 27C16 EPROM and 6116 RAMs are also included on the board.

BOARD ADDRESS

The default address of the board is 2000H - 2FFFH in memory space (and 20H to 2FH in I/O space), but it can be re-addressed to any of seven other memory (and I/O) locations: 0 - 0FFFH (0 - 0FH), 1000H - 1FFFH (10H-1FH), 3000H - 3FFFH (30H - 3FH), 8000H - 8FFFH (80H - 8FH), 9000H - 9FFFH (90H - 9FH), 0A000H - 0AFFFH (0A0H - 0AFH),or 0B000H - 0BFFFH (0B0H - 0BFH). The board is re-addressed by moving a jumper in the address definition area at the bottom of the board.

These addresses refer to the system address space, which corresponds to normal memory space for the CPU-800A or CPU-8085, but not for the CPU-6805A. Since the 6805E2 has only 8K of address space <u>in total</u>, to gain it 32K of off-board address space it was necessary to provide bank switching for that part of the 6805E2's address space that is assigned to off-board use. This 4K block (seen as 800H to 17FFH by the 6805E2), appears as eight blocks (8000H - 8FFFH, 9000H - 9FFFH up to 0F000H - 0FFFFH) off-board the CPU-6805A, depending upon the setting of the bank-switching lines. Accordingly when used with the CPU-6805A, the MOR-800 must be addressed in the upper half of memory space (8000H or above). Port space will appear in the address range 80H to 0FFFH, depending upon how the board is addressed.

In subsequent discussions of port addressing, the default board address of 2000H - 2FFFH will be assumed for systems using the CPU-800A or CPU-8085, and 8000H to 8FFFH for systems using the CPU-6805A.

ON-BOARD ADDRESS SPACE

In the table below are shown the port and memory assignments for the MOR-800 card. The default address of 2000H is assumed for CPU-800A or CPU-8085 based systems, and 8000H is assumed for CPU-6805A based systems. Reassigning the board address will affect only the most significant bit of the port or memory address for CPU-800A and CPU-8085 based systems, the bank number, and the most significant bit of the 'port' space's address for CPU-6805A based systems. The RAM and EPROM sockets are interchangable. The board is shipped with the parts installed as shown below.

ADDRESS CPU-800A	ADDRESS CPU-6805A	FUNCTION READ	WRITE
2000H-203FH	-----*	RTC	RTC
2200H-27FFH	800-0FFF (BANK 0)	6116 RAM	6116
2800H-2FFFH	1000-17FF (BANK 0)	EPROM	---
20H	80H	A TO D STATUS	A TO D CNTRL
21H	81H	MSB RESULT	------
22H	82H	LSB RESULT	------
28H	88H	-EOC**	POWER
***			

* Systems not using the RTC can provide the 6116 RAM with a full 2K of address space by making a cut and jump in the jumper space below and to the right of the 7002 converter. Details of this are given in the 6116 RAM discussion below.

** NEC claims that reading the 7002 converter while a conversion is in progress adds to the conversion's uncertainty. Accordingly, the converter's -EOC output has been made available at a port separate from the 7002. If the end of conversion is awaited by looping on a flag, use this port. Both bits 7 and 0 of this port give -END OF CONVERSION (the '-'is used to indicate negative true).

*** Bits 7 and 0 are used to provide the power switching to the converter. Bit 7 controls the power, while bit 0 enables the control lines to the converter. When powering up the converter, first apply power by writing a 1 to bit 7, and then after at least 6 mS connect the control lines by writing a 1 to bit 0.

D7 D6 D5 D4 D3 D2 D1 D0

input Channel

0 = 8bit
1 = 12bit

A TO D CONVERTER INTERFACE

The MOR-800 uses an NEC 7002 4-channel converter. Although this part makes 12-bit conversions, it has an accuracy and repeatablility of about 10-bits. The chip has an on-board multiplexer and can be programmed to make 8-bit or '10-bit' conversions of any of the four input channels by writing the appropriate command word to the control port. Bits D0 and D1 of the command word specify the input channel, and D3 specifies the conversion accuracy (8-bit=0, 12-bit=1). The other bits of the word are ignored. Conversion time for a 12-bit conversion is typically 10 mS with a 1 MHz input clock rate and 4 mS for an 8-bit conversion.

CONTROL = 20

An LM-236 is used as a voltage reference. When the board is tested the reference is adjusted to 2.500 volts giving the converter an input range of 0 to 2.5 volts. Typical linearity and accuracy is 0.1% of full scale.

POWER-SWITCHED CONVERTER

In order to meet the C-44 bus power consumption specification it was necessary to add power switching circuitry to the converter. The converter interface is fully buffered, allowing this section to be powered down completely.

Two bits (D7 and D0) of the POWER port control powering the converter up and down. Since the converter is CMOS, the power line must be brought up before the control lines are enabled. This powering up sequence must be followed to prevent the possibilty of SCR latchup in the converter.

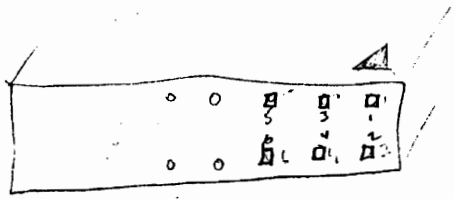
1) Write 80H to the POWER PORT (port address 28H for CPU-800A or CPU-8085, memory address 88H for CPU-6805A) to enable power to the display.
2) Wait at least 6 milliseconds to let the voltage settle.
3) Write 81H to the POWER PORT to enable the data and control lines.

At this point the converter will be powered and can receive commands; however, the converter's supply lines will have not quite reached their steady state values. It is a good idea to make one conversion after power up to settle the converter before using it in earnest.

26-PIN CONNECTOR

The A to D Converter inputs are brought to a 26-pin ribbon cable connector along with ground, common, and switched Vreg. The ribbon cable is numbered sequentially from the left end facing the board. The connector pins are numbered to correspond to the wires in the cable. All even numbered pins are ground.

PIN	FUNCTION
1	Switched Vreg
3	COMMON
5	CHAN 3
7	Switched Vreg
9	COMMON
11	CHAN 2
13	Switched Vreg
15	COMMON
17	CHAN 1
19	Switched Vreg
21	COMMON
23	CHAN 0
25	-----



REAL TIME CLOCK

The MOR-800 can optionally have a 6818 real-time clock (RTC). In our implementation, the 6818 uses a 32.768 KHz crystal which has a stability of about 20 ppm over the temperature range 0 to 50 degrees C. The RTC can be programmed to provide interrupts at intervals as short as 3.2 milliseconds, or as long as once per day. Interrupt rates greater than once per second are set by using the periodic interrupt capability of the 6818 RTC, and are binary submultiples of 1 second. Interrupt intervals one second or greater are programmed by setting the time at which the next interrupt is to occur.

The RTC is addressed at 2000H to 203FH, although the address decoding circuit allocates it a much larger space (2000H to 21FFH). The details of the operation of the RTC are described in the accompaning 6818 manual.

The board is available without the RTC for use with the CPU-6805A, or in applications that do not require an RTC. In that case, the memory space taken by the RTC can be allocated to the 6116 RAM to give it a full 2K memory space.

ADDITIONAL RAM

The MOR-800 provides additional system RAM in the form of a 6116 2K RAM chip. When the board comes without an RTC, the 6116 can be allocated a full 2K of address space (2000H to 27FFH), but systems requiring the RTC will only have 1.5K available (2200H to 27FFH). The 6116 RAM is not fully CMOS and therefore draws a substantial amount of current when it is accessed.

The two 24 pins sockets are wired identically so that they can be used either for RAM or EPROM as the application demands.

The jumper area that determines the allocation of address space between RAM and RTC is directly below the 3K resistor below and to the right of the 7002 converter chip. There are three pads in this area. With the outside two connected the RTC is allocated 1/4 of the address space and the RAM the rest. To allocate the entire address space to the RAM, the etch connecting these outside pads should be cut, and the rightmost two should be connected instead.

POWER CONSUMPTION

Typical current drains for the MOR-800 operating with a CPU-800A are shown in the table below. When used with a CPU-6805A the board (without RTC) draws less than 30 microamps in its powered down state.

A TO D	MODE	BATTERY	Vreg
ON	ACTIVE	3 mA	8.5 mA
OFF	ACTIVE	<0.01 mA	1.0 mA
OFF	STOP (HYB)	<0.01 mA	0.2 mA
(WITHOUT REAL TIME CLOCK)			
ON	ACTIVE	3 mA	8.2 mA
OFF	ACTIVE	<0.01 mA	0.7 mA
OFF	STOP (HYB)	<0.01 mA	<0.03 mA

USING AN INTERRUPT

The RTC's - IRQ output is connected to the INT A line (PIN F) so that sleep-wake control can be handled by this line. If the board has no RTC installed this will have no effect. If the RTC is installed, but this interrupt feature is not desired, it can be defeated by cutting an etch near the bottom of the card. Alternatively the interrupt can be connected to the INT B or WAKEUP lines of the bus.

A FULLY BUFFERED BUS

Thanks to the recent introduction of TTL compatible CMOS buffer chips, it has been possible to provide complete buffering of the address, data and control lines coming from the MOR-800. This keeps the capacitive loading of the bus low, permitting at least 10 memory and/or port expansion boards per system without causing excessive skew.

THE HYBERNATE MODE

C-44 bus CPU's have low power modes that reduce the Vreg supply voltage to about 3.0 volts. Since the MOR-800's 5 volt supply comes from this source, the board sees a reduced supply during the HYBERNATE states of these CPU's. This is not a problem for any of the parts on the board.

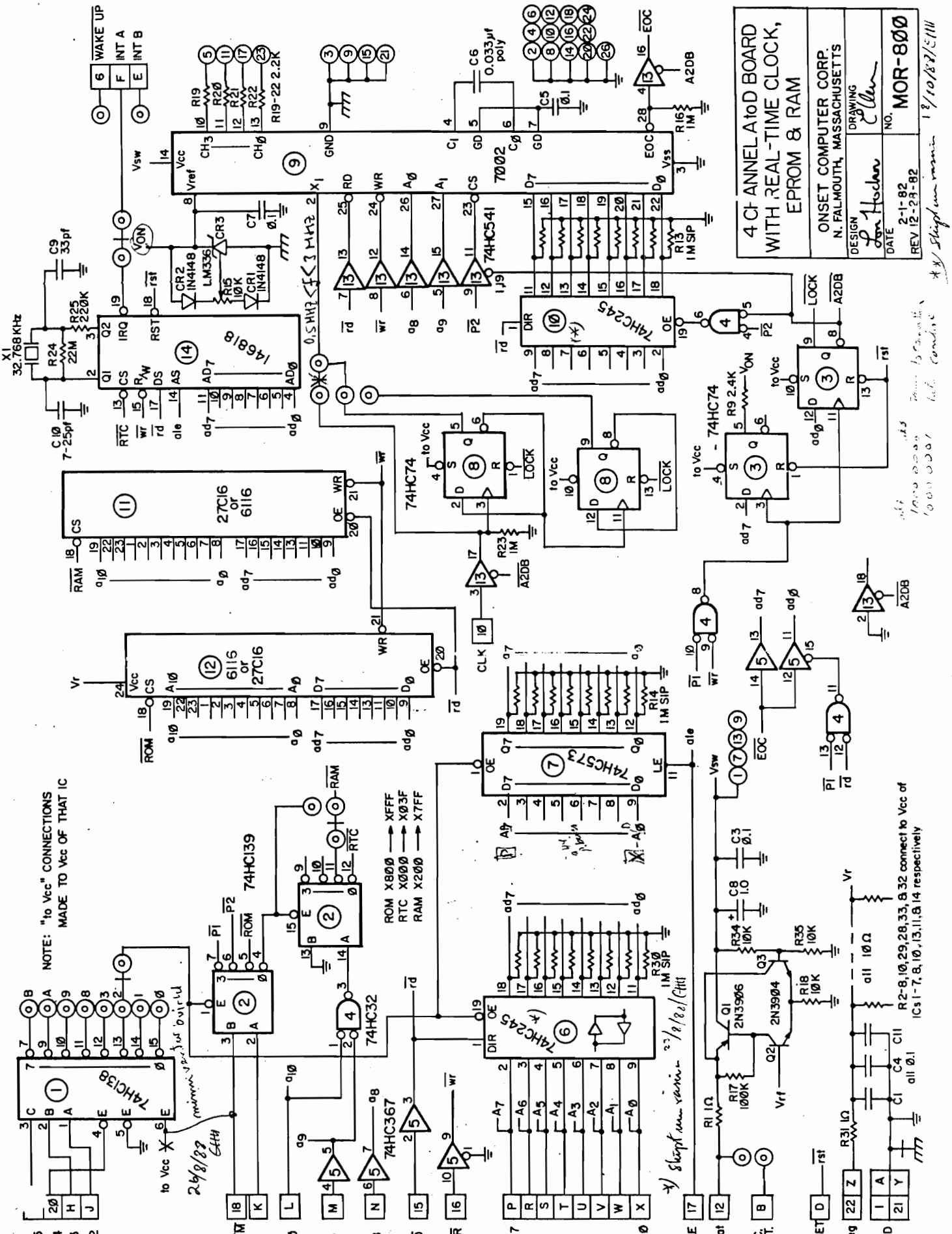
CHECKING THE CURRENT DRAIN

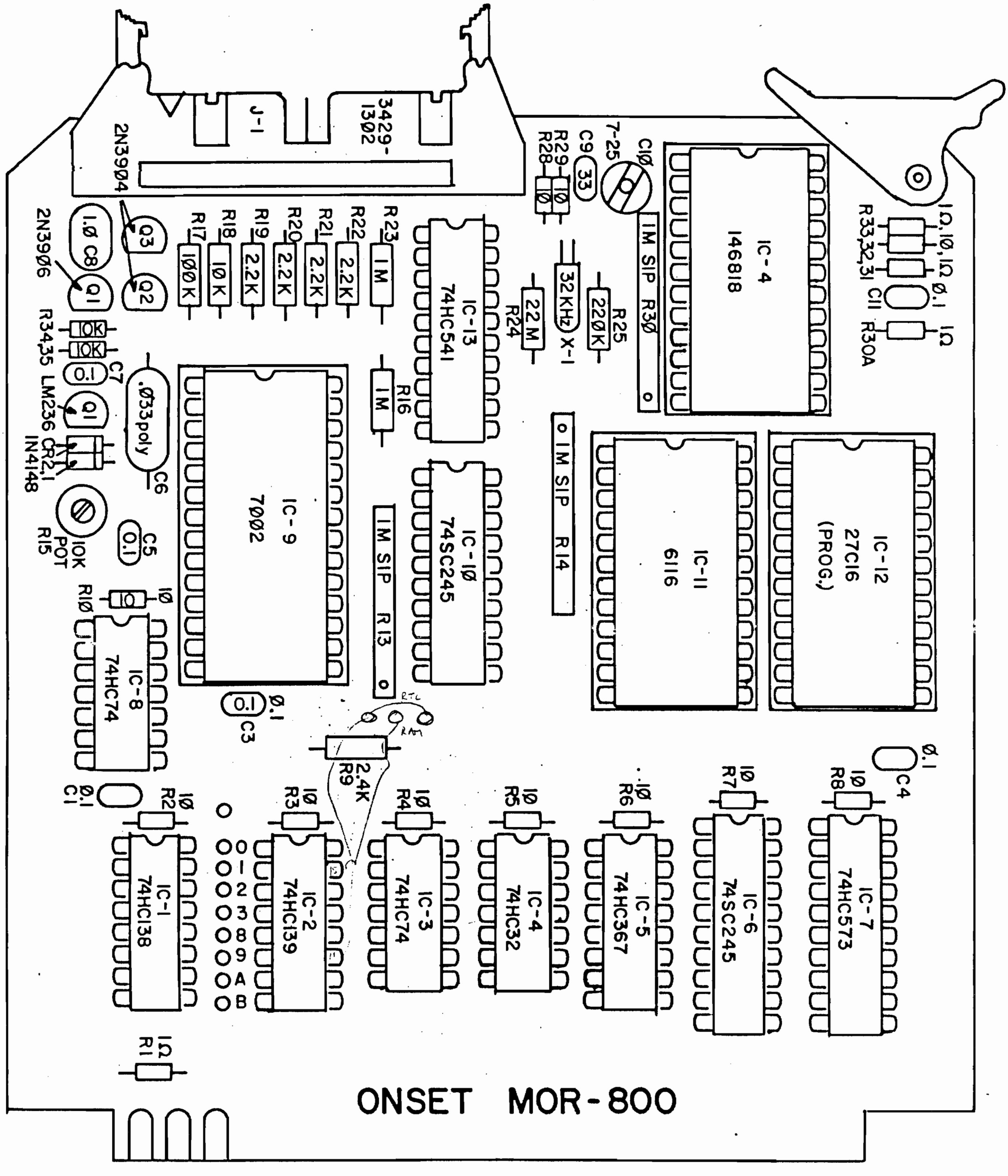
There are current sensing resistors for all IC's on the MOR-800. These resistors make it possible to measure the current usage of the IC's during checkout, and greatly simplify tracking down failures. Board current sense resistors allow monitoring current usage from both the regulated 5 volt supply and the battery supply.

CARD EDGE CONNECTION FOR THE MOR-800

The definition of the pins used by the MOR-800 are shown below; they are totally compatible with the C-44 bus. A minus sign preceding a signal indicates that its active level is negative. N.C. indicates that no connection is made to that line.

(COMPONENT SIDE)		(SOLDER SIDE)	
(1)	GROUND	(A)	GROUND
(2)	N.C.	(B)	H.C. BATTERY
(3)	N.C.	(C)	N.C.
(4)	N.C.	(D)	-RESET OUT
(5)	N.C.	(E)	-INT B
(6)	-WAKEUP	(F)	-INT A
(7)	N.C.	(H)	A13
(8)	N.C.	(J)	A12
(9)	N.C.	(K)	A11
(10	CLOCK	(L)	A10
(11)	N.C.	(M)	A9
(12)	BATTERY	(N)	A8
(13)	N.C.	(P)	AD7
(14)	N.C.	(R)	AD6
(15)	- READ	(S)	AD5
(16)	- WRITE	(T)	AD4
(17)	ALE	(U)	AD3
(18)	IO/-M	(V)	AD2
(19)	A15	(W)	AD1
(20)	A14	(X)	AD0
(21)	GROUND	(Y)	GROUND
(22)	Vreg	(Z)	Vreg


4 CHANNEL A to D BOARD WITH REAL-TIME CLOCK, EPROM & RAM
ONSET COMPUTER CORP.
N. FALMOUTH, MASSACHUSETTS
DESIGN
DRAWING
DATE 2-1-82
REV 12-29-82
NO. MOR-800
NOTE: "to Vcc" CONNECTIONS MADE TO Vcc OF THAT IC
ROM X800 — XFFF
RTC X000 — X03F
RAM X200 — X7FF
R2-8, 10, 29, 28, 33, & 32 connect to Vcc of ICs 1-7, 8, 10, 13, 11, & 14 respectively
74HC138
74HC139
74HC32
74HC367
74HC245
74HC573
74HC74
74HC541
7002
6116 or 27C16
6818
WAKE UP
INT A
INT B
X1 32.768 KHz
LM336
IN4148
LOCK
RESET
Vreg
GND
Vbat
ALE
A2D8
EOC



ONSET MOR-800
J-1
3429-1302
2N39Ø4
2N39Ø6
IC-1 74HC138
IC-2 74HC139
IC-3 74HC74
IC-4 74HC32
IC-5 74HC367
IC-6 74SC245
IC-7 74HC573
IC-8 74HC74
IC-9 7ØØ2
IC-1Ø 74SC245
IC-11 6116
IC-12 27C16 (PROG.)
IC-13 74HC541
IC-4 146818
1M SIP R13
1M SIP R14
1M SIP R3Ø
32KHz X-1
LM236
1N4148
10K POT R15
.Ø33poly C6

NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μPD7002

10-BIT BINARY A/D CONVERTER

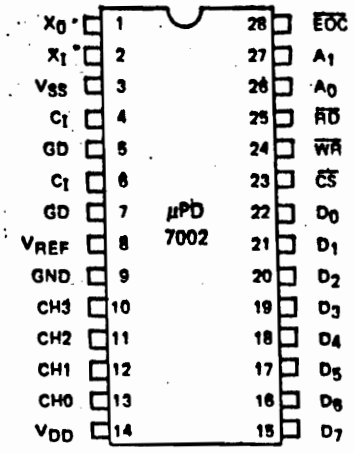
DESCRIPTION

The μPD7002 is a high performance, low power, monolithic CMOS A/D converter designed for microprocessor applications. The analog input voltage is applied to one of the four analog inputs. By loading the input register with the multiplexer channel and the desired resolution (8 or 10 bits) the integrating A/D conversion sequence is started. At the end of conversion $\overline{EOC}$ signal goes low and if connected to the interrupt line of microprocessor it will cause an interrupt. At this point the digital data can be read in two bytes from the output registers. The μPD7002 also features a status register that can be read at any time.

FEATURES

- Single Chip CMOS LSI
- Resolution: 8 or 10 Bits
- 4 Channel Analog Multiplexer
- Auto-Zeroscale and Auto-Fullscale Corrections without any External Components
- High Input Impedance: 1000MΩ
- Readout of Internal Status Register Through Data Bus
- Single +5V Power Supply
- Interfaces to Most 8-Bit Microprocessors
- Conversion Speed: 5 ms (10 Bit, f_{CK} = 2 MHz)
- Power Consumption: 15 mW
- Available in a 28 Pin Plastic Package
- 2 Performance Ranges
  Conversion Accuracy (Max) T_a = 0° to 50°C
  μPD7002C-1; 0.1% FSR
  μPD7002C ; 0.2% FSR

PIN CONFIGURATION



PIN NAMES

X_0,X_I	External Clock Input
V_{SS}	TTL Ground
C_I	Integrating Capacitor
GD	Guard
V_{REF}	Reference Voltage Input
GND	Analog Ground
CH3	Analog Channel 3
CH2	Analog Channel 2
CH1	Analog Channel 1
CH0	Analog Channel 0
V_{DD}	TTL Voltage (+5V)
D_0-D_7	Data Bus
$\overline{CS}$	Chip Select
$\overline{WR}$, $\overline{RD}$	Control Bus
A_0,A_1	Address Bus
$\overline{EOC}$	End of Conversion Interrupt

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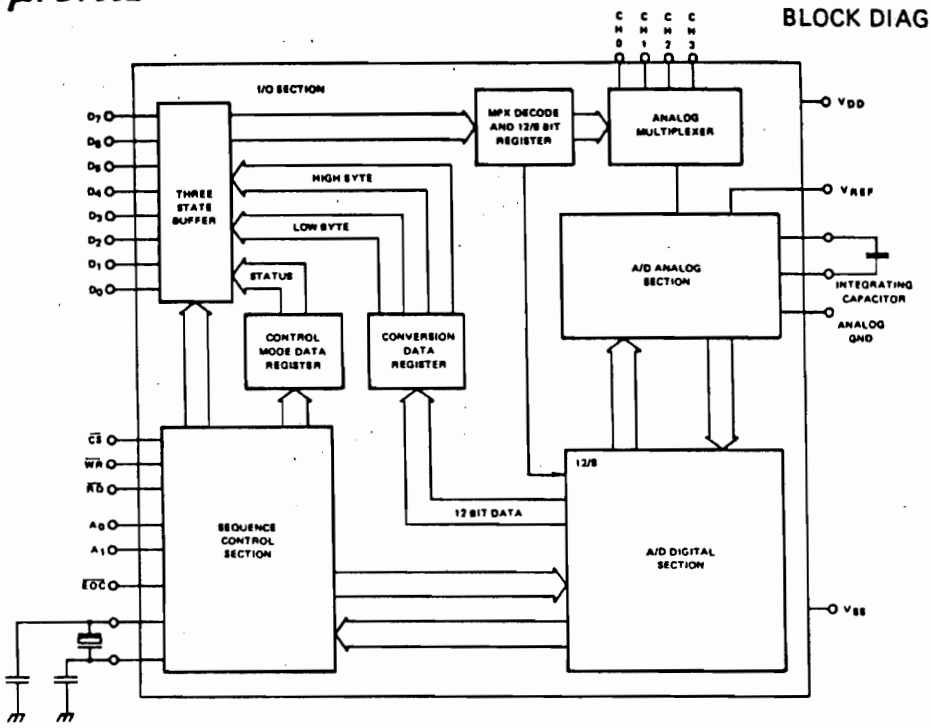
μPD7002

BLOCK DIAGRAM



DC CHARACTERISTICS

T_a 0 to 50°C; V_{DD} = +5 ±0.25V, V_{REF} = +2.50V, f_{CK} = 1 MHz

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Resolution	7002C-1		10	11	12	Bits	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C		9	11	12		
Non Linearity	7002C-1			0.05	0.1	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C			0.1	0.2		
Fullscale Error	7002C-1			0.05	0.1	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C			0.1	0.2		
Zeroscale Error	7002C-1			0.05	0.1	%FSR	V_{DD} = 5V, V_{REF} = 2.5 ± 0.25V
	7002C			0.1	0.2		
Fullscale Temperature Coefficient				10		PPM/°C	V_{DD} = 5V
Zeroscale Temperature Coefficient				10		PPM/°C	V_{DD} = 5V
Analog Input Voltage Range		V_{IA}	0		V_{REF}	V	
Analog Input Resistance		R_{IA}		1000		MΩ	V_{IA} = V_{SS} to V_{DD}
Total Unadjusted Error 1	7002C-1	T.U.E. 1		0.05	0.1	%FSR	V_{REF} = 2.25 to 2.75V, V_{DD} = 5V
	7002C	T.U.E. 1		0.1	0.2		
Total Unadjusted Error 2	7002C-1	T.U.E. 2		0.05	0.1	%FSR	V_{REF} = 2.5V, V_{DD} = 4.75 to 5.25V
	7002C	T.U.E. 2		0.1	0.2		
Clock Input Current		I_{XI}		5	50	μA	
Clock Input High Level		V_{XIH}	V_{DD}-1.4			V	
Clock Input Low Level		V_{XIL}			V_{SS}+1.4	V	
High Level Input Voltage		V_{IH}	2.2			V	T_a = -20°C to +70°C
Low Level Input Voltage		V_{IL}			0.8	V	T_a = -20°C to +70°C
High Level Output Voltage		V_{OH}	V_{DD}-1.5			V	I_O = -1.6 mA, T_a = -20°C to +70°C
Low Level Output Voltage		V_{OL}			0.45	V	I_O = +16 mA, T_a = -20°C to +70°C
Digital Input Leakage Current		I_I		1	10	μA	V_I = V_{SS} to V_{DD}
High-Z Output Leakage Current		I_{Leak}		1	10	μA	V_O = V_{SS} to V_{DD}
Power Dissipation		Pd		15	25	mW	f_{CK} ≤ 1 MHz

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... -20°C to +70°C
Storage Temperature ..... -65°C to +150°C
All Input Voltages ..... -0.3 to V_{DD} + 0.3 Volts
Power Supply ..... -0.3 to +7 Volts
Power Dissipation ..... 300 mW
Analog GND Voltage ..... V_{SS} ± 0.3 Volts
T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

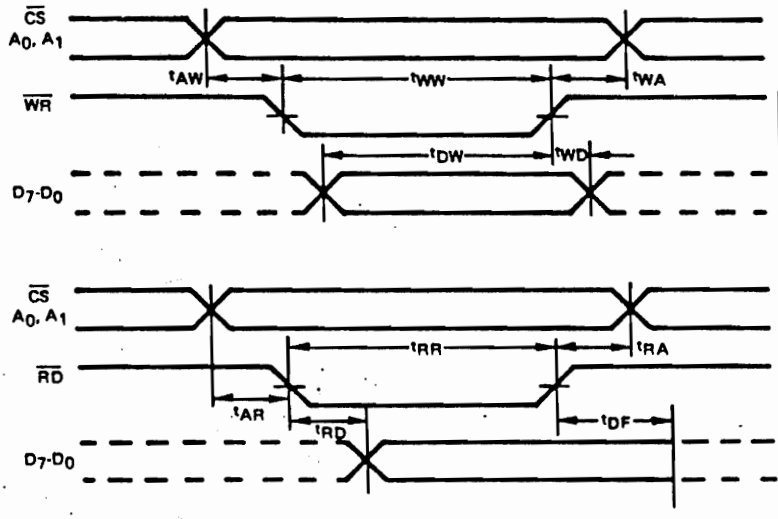
AC CHARACTERISTICS

T_a = 25° ± 2°C; V_{DD} = +5 ± 0.25V; V_{REF} = 2.5V; f_{CK} = 1 MHz; C_{INT} = 0.033 μF

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Conversion Speed (12 bit)	t_{CONV}	8.5	10	15	ms	f_{CK} = 1 MHz
Conversion Speed (8 bit)	t_{CONV}	2.4	4	5	ms	f_{CK} = 1 MHz
Clock Frequency Range	f_{CK}	0.5	1	3	MHz	
Integrating Capacitor Value	C_{INT}*	0.029			μF	V_{REF} = 2.50V, f_{CK} = 1 MHz
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{WR}$	t_{AW}	50			ns	
Address Setup Time $\overline{CS}$, A_0, A_1, to $\overline{RD}$	t_{AR}	50			ns	
Address Hold Time $\overline{WR}$ to CS, A_0, A_1	t_{WA}	50			ns	
Address Hold Time $\overline{RD}$ to CS, A_0, A_1	t_{RA}	50			ns	
Low Level $\overline{WR}$ Pulse Width	t_{WW}	400			ns	
Low Level $\overline{RD}$ Pulse Width	t_{RR}	400			ns	
Data Setup Time Input Data to $\overline{WR}$	t_{DW}	300			ns	
Data Hold Time $\overline{WR}$ to Input Data	t_{WD}	50			ns	
Output Delay Time $\overline{RD}$ to Output Data	t_{RD}			300	ns	1TTL + 100 pF
Delay Time to High Z Output $\overline{RD}$ to Floating Output	t_{DF}			150	ns	

* $C_{INT}(\mu F)(Min) = 0.029/f_{CK}(MHz)$

TIMING WAVEFORMS



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μPD7002

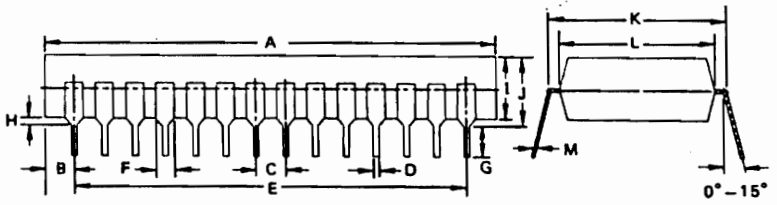
CONTROL TERMINAL FUNCTIONS

CONTROL TERMINALS					MODE	INTERNAL FUNCTION	DATA INPUT-OUTPUT TERMINALS
$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0			
H	x	x	x	x	Not selected		High impedance
L	H	H	x	x	Not selected	–	
L	H	L	L	L	Write mode	Data latch A/D start	Input status, D_1, D_0 = MPX address D_3 = 8 bit/10 bit conversion designation. ① D_2 = Flag Input
L	H	L	L	H	Not selected	–	High impedance
L	H	L	H	L	Not selected	–	
L	H	L	H	H	Test mode	Test status	Input status ②
L	L	H	L	L	Read mode	Internal status	D_7 = $\overline{EOC}$, D_6 = $\overline{BUSY}$, D_5 = MSB, D_4 = 2nd MSB, D_3 = 8/10, D_2 = not used D_1 = MPX, D_0 = MPX
L	L	H	L	H	Read mode	High data byte	D_7-D_0 = MSB – 8th bit
L	L	H	H	L	Read mode	Low data byte	D_7-D_4 = 9th – 10th bit, D_3-D_0 = L
L	L	H	H	H	Read mode	Low data byte	

Notes: ① Designation of number of conversion bits: 8 bit = L; 10 bit = H.

② Test Mode: Used for inspecting the device. The data input-output terminals assume an input state and are connected to the A/D counter. Therefore, the A/D conversion data read out after this is meaningless.

PACKAGE OUTLINE μPD7002C



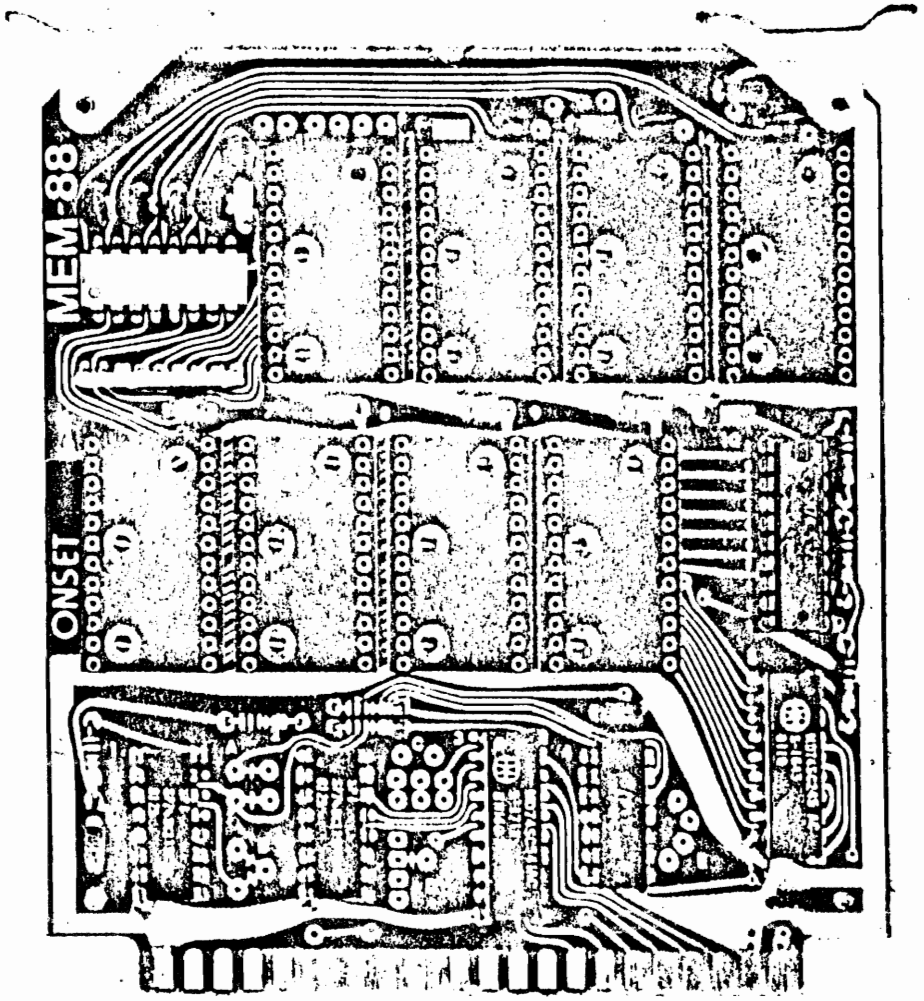
PLASTIC

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

VIÐAUKI G

Minnisbretti

The MEM-88 Manual



ONSET
Computer Corp.
199 Main St.
P.O. Box 1016
N. Falmouth, MA 02556

February 1983

MEM-88

CMOS MEMORY EXPANSION BOARD

FEATURES:

* SOCKETS FOR 27C16 EPROMS OR 6116 RAM CHIPS
* FULLY BUFFERED INTERFACE
* JUMPER ADDRESSABLE TO ANY OF 4 LOCATIONS
* <100 MICROAMP DRAIN WHEN NOT ACCESSED
* C-44 BUS COMPATIBILITY

INTRODUCTION

The MEM-88 is a memory expansion board for the C-44 bus. The board has eight 24-pin sockets which can be used to hold 6116 RAM chips or 27C16 chips. The board can be stuffed with any mix of EPROM and RAM without modification. This 16K memory board can be addressed to any of four memory blocks.

RAM

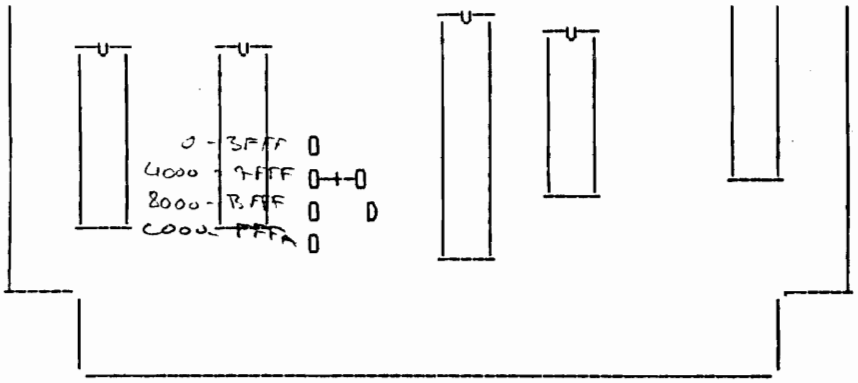
The MEM-88 takes advantage of the new 24-pin RAM chips from Toshiba, Hitachi and other makers. The Hitachi 6116-L4 is recommended for RAM as this inexpensive part will contribute negligibly to the current drain of the system.

27C16 EPROMS

The speed of the 27C16 EPROMs should be chosen to give the appropriate access time for your system. 450 nS parts are reccommended for CPU-6805A, CPU-8085 and CPU-800A based systems, while 650 nS parts are more than adequate for the CPU-800A-1.

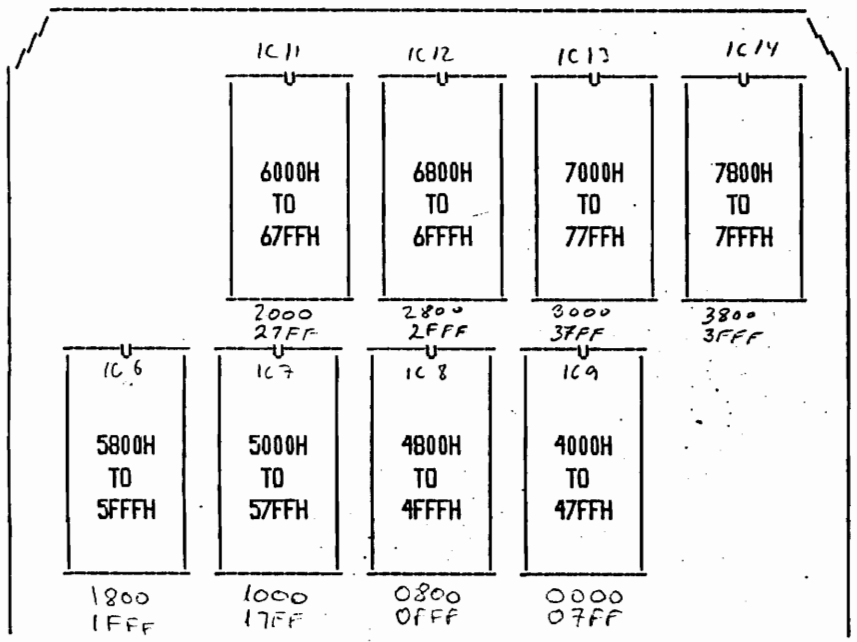
ADDRESS DECODING

The MEM-88 has a default address of 4000H to 7FFFH. By changing the jumper selection in jumper area D, the board can be re-addressed. Connecting to the top pad in the group addresses the board to 0-3FFFH; the second pad down (default address) addresses the board to 4000-7FFFH. The last two pads going down select the address ranges 8000H-BFFFH and C000H-FFFFH respectively.



THE MEMORY LOCATION MAP

The figure below shows the memory address for the sockets of the board assuming the default board address.



POWER CONSUMPTION

The typical power consumption of the MEM-88 is a strong function of the operating mode, as shown in the table below.

MODE	BATTERY SUPPLY	CURRENT DRAIN
NOT ACCESSED	5 VOLTS	<0.1 mA
NOT ACCESSED	3 VOLTS	<0.03 mA
27C16 ROM ACCESSED	5 VOLTS	20 mA
6116 RAM ACCESSED	5 VOLTS	40 mA

A FULLY BUFFERED BUS

Thanks the introduction of octal CMOS buffer chips, it has been possible to provide complete buffering of the address, data and control lines coming from the MEM-88. This keeps the capacitive loading of the bus low, permitting at least 10 memory and/or port expansion boards per system without causing excessive skew.

THE HYBERNATE MODE

C-44 bus CPU's have low power modes that reduce the Vreg supply voltage to about 3.0 volts. Since the MEM-88's positive supply comes from this source, the board sees a reduced supply during the HYBERNATE states of these CPU's. The board will properly retain voltage in this reduced voltage mode if appropriate RAM chips are installed. The 6116-L has guaranteed 2.0 volt data retention.

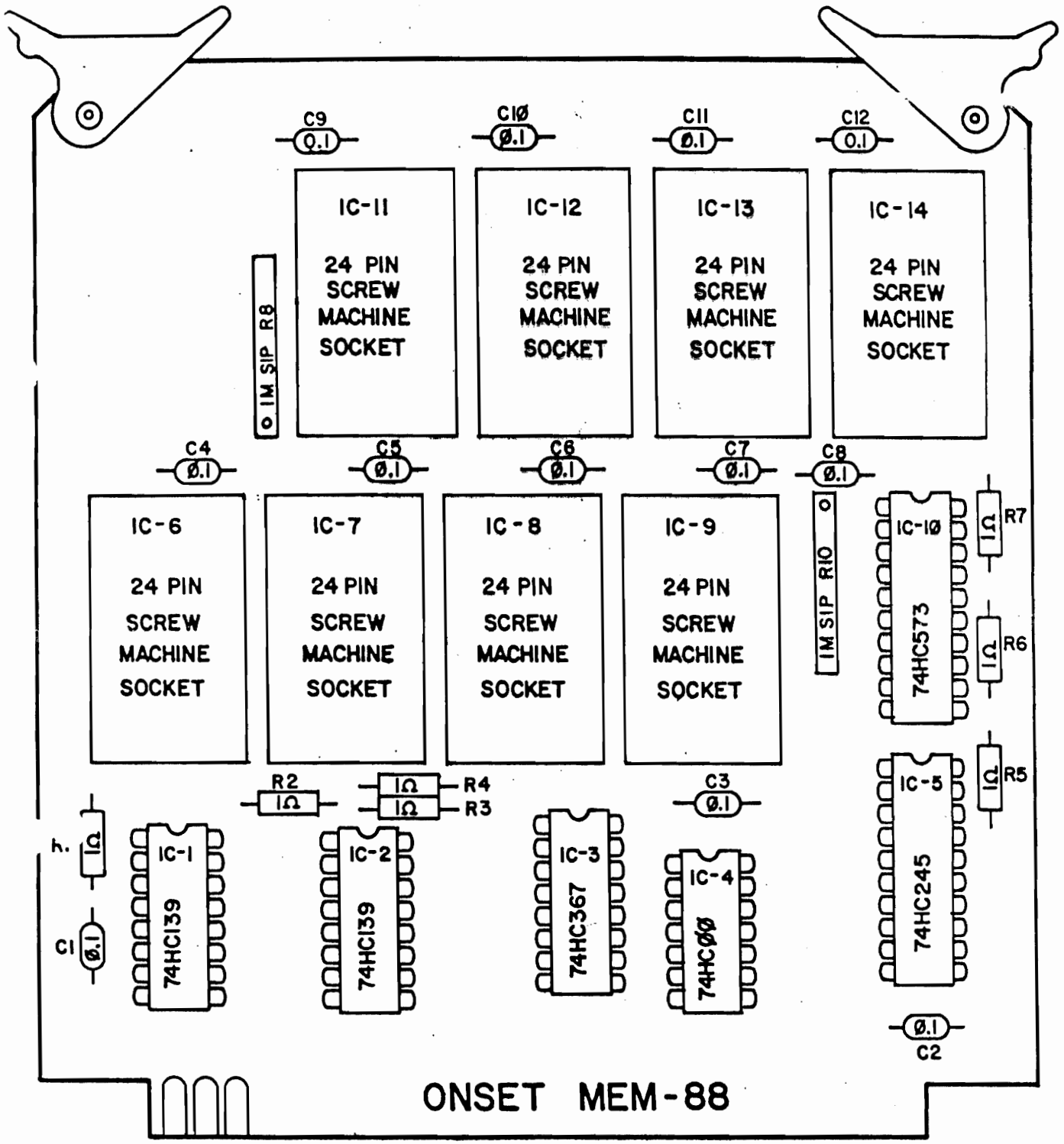
CHECKING THE CURRENT DRAIN

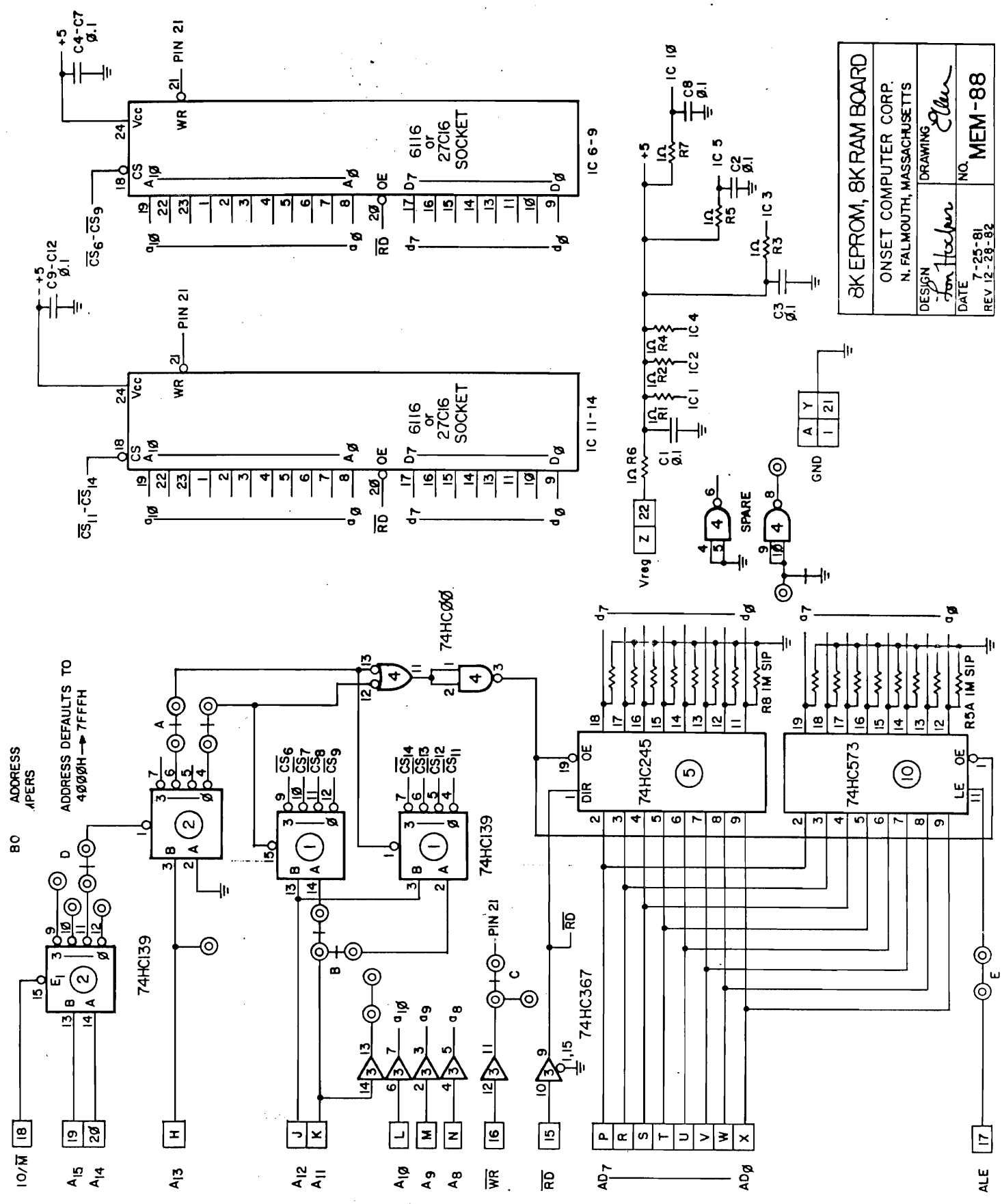
There are seven one-ohm current sensing resistors on the MEM-88. These resistors allow sensing the current drain of the whole board and each of the decode and buffer chips. Since the RAM and EPROM chips are mounted in sockets, and they can be removed without leaving any uncommitted CMOS inputs on the board, sense resistors are not necessary for these parts.

CARD EDGE CONNECTION FOR THE MEM-88

The definitions of the pins used by the MEM-88 are shown below; they are totally compatible with the C-44 bus. A minus sign preceding a signal indicates that its active level is negative. N.C. indicates that no connection is made to that line.

(COMPONENT SIDE)		(SOLDER SIDE)	
(1)	GROUND	(A)	GROUND
(2)	N.C.	(B)	N.C.
(3)	N.C.	(C)	N.C.
(4)	N.C.	(D)	N.C.
(5)	N.C.	(E)	N.C.
(6)	N.C.	(F)	N.C.
(7)	N.C.	(H)	A13
(8)	N.C.	(J)	A12
(9)	N.C.	(K)	A11
(10	N.C.	(L)	A10
(11)	N.C.	(M)	A9
(12)	N.C.	(N)	A8
(13)	N.C.	(P)	AD7
(14)	N.C.	(R)	AD6
(15)	- READ	(S)	AD5
(16)	- WRITE	(T)	AD4
(17)	ALE	(U)	AD3
(18)	IO/-M	(V)	AD2
(19)	A15	(W)	AD1
(20)	A14	(X)	AD0
(21)	GROUND	(Y)	GROUND
(22)	Vreg	(Z)	Vreg


C9 0.1
C10 0.1
C11 0.1
C12 0.1
IC-11
24 PIN SCREW MACHINE SOCKET
IC-12
24 PIN SCREW MACHINE SOCKET
IC-13
24 PIN SCREW MACHINE SOCKET
IC-14
24 PIN SCREW MACHINE SOCKET
1M SIP R8
C4 0.1
C5 0.1
C6 0.1
C7 0.1
C8 0.1
IC-6
24 PIN SCREW MACHINE SOCKET
IC-7
24 PIN SCREW MACHINE SOCKET
IC-8
24 PIN SCREW MACHINE SOCKET
IC-9
24 PIN SCREW MACHINE SOCKET
1M SIP R10
IC-10
74HC573
1Ω R7
1Ω R6
1Ω R5
R2 1Ω
1Ω R4
1Ω R3
C3 0.1
IC-1
74HC139
IC-2
74HC139
IC-3
74HC367
IC-4
74HC00
IC-5
74HC245
C1 0.1
C2 0.1
ONSET MEM-88


8K EPROM, 8K RAM BOARD
ONSET COMPUTER CORP.
N. FALMOUTH, MASSACHUSETTS
DESIGN
DRAWING
DATE 7-25-81
REV 12-28-82
NO. MEM-88
IC 6-9
IC 11-14
6116 or 27C16 SOCKET
PIN 21
C4-C7 .1
C9-C12 .1
C1 .1
C2 .1
C3 .1
C8 .1
R1
R2
R3
R4
R5
R6
R7
IC 1
IC2
IC 3
IC 4
IC 5
IC 10
SPARE
GND
Vreg
74HC00
74HC139
74HC367
74HC245
74HC573
R8 1M SIP
R5A 1M SIP
ADDRESS DEFAULTS TO 4000H → 7FFFH
ADDRESS JUMPERS
IO/M
ALE

VIÐAUKI H

Bæklingur um móttakara

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

INSTRUCTION MANUAL

UHF NBFM RECEIVER

MODEL R45F

(400-475MHz)

July 1986

Monitron Corporation
P.O. Box 27485
Tulsa, OK 74149-0485
(918) 836-6831

MODEL R 45 F S/N 1251 469.500 MHz

FINAL TEST DATA

+25°C Ein 13.8 VDC; Iin 17 ma.

S+N/N @ 1 microvolt (1KHz Mod; 5KHz Dev): 27 db.

Modulation response (10 microvolts RF Input):

Mod.Freq.	Dev.	Audio (600 ohms)	Distortion
300 Hz.	KHz.	0 dbm	
* 1000 Hz.	5.0 KHz.	0 dbm	0.8 %
3000 Hz.	KHz.	-0.3 dbm	

Squelch ✓; Voltage Regulator 9.62 VDC ; *=Reference

-30°C Ein 13.8 VDC; Iin 17 ma.

S+N/N @ 1 microvolt (1KHz Mod; 5KHz Dev): 27.5 db.

Audio Output (10 microvolts; 1KHz Mod; 5KHz Dev): +1.3 dbm; Dist.=1.5 %

+60°C Ein 13.8 VDC; Iin 17 ma.

S+N/N @ 1 microvolt (1KHz Mod; 5KHz Dev): 26 db.

Audio Output (10 microvolt; 1KHz Mod; 5KHz Dev); -1.2 dbm; Dist.=1.1 %

Final acceptance: MBR

Date: 12-21-87

Notes:

Pin Connections

A = +13.8VDC
B = Audio Output
C = ~~Signal~~ Strength
D = Ground

INDEX

RECEIVER

GENERAL DESCRIPTION

The Monitron Model R45F is an all solid-state, narrowband, FM receiver designed to provide superior reception of signals in the 400-475MHz UHF band.

In addition to its excellent sensitivity, selectivity, and wide dynamic operating range, every effort has ben made to maintain very low distortion of the recovered audio signal, along with an essentially flat frequency response over the modulation bandwidth. These qualities are maintained throughout the operating temperature range.

Only quality components are used in the manufacture of the receiver; these are mounted on a single-sided glass printed circuit board. Most components are visible upon removal of the cover and all parts are readily accessible for test or replacement.

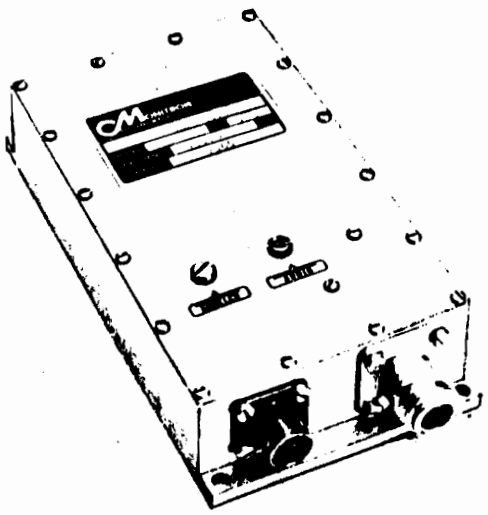
The receiver is housed in a thick-walled aluminum alloy box, machined from a single piece of bar stock. This results in a seamless, almost indestructible housing which is RF "tight" and impervious to the environment.

These salient features--technical excellence, quality of manufacture, reliability and durability--make these receivers ideal for those engaged in telemetering scientific data.

Monitron also manufactures a series of NBFM UHF transmitters designed as companion units for the above receiver, as well as a complete line of VHF equipment.

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

UHF TELEMETRY RECEIVER



MODEL R45F

- **NBFM — ANALOG OR DIGITAL DATA**
- **HIGH RELIABILITY — 100% TESTED**
- **MILITARY QUALITY — EXTREMELY RUGGED**
- **COMPLETE PERFORMANCE SPECIFICATIONS**
- **LOW POWER REQUIREMENT**
- **1 YEAR WARRANTY**

SPECIFICATIONS — MODEL R45F

GENERAL

Receiver Type:
Frequency Modulation (Narrow-Band FM)
Dual-conversion, solid-state design
Frequency Range:
400-470 MHz; factory preset to any frequency in this band.
(Other frequencies available).

ELECTRICAL

Input Power:
11 to 15 Vdc @ 20 mA typical (25 mA maximum)
Power Protection:
Protected against reversed supply polarity;
Internally regulated
RF Input Impedance:
50 ohms
Frequency Response:
300 to 3000 Hz minimum
± 0.5% dB typical, ± 1.5 dB maximum
Operating Dynamic Range:
RF input — 113 dBm to 0 dBm minimum
(0.5 μV to 0.22 V)
Sensitivity (S + N/N), 5 kHz deviation:
25 dB typical @ 1 μV
10 dB minimum @ 0.5 μV
Selectivity:
8-pole monolithic band pass filter at first IF;
60 dB @ ± 30 kHz; 80 dB @ ± 40 kHz
Stability:
± 0.001 % of center frequency, −30° to 60°C
Spurious and Image Rejection:
More than 50 dB below signal response
Modulation Acceptance:
± 7 kHz, minimum
Audio Output:
0 to + 6 dBm (600 ohms), ± 1.5 db. continuously adjustable
Audio Distortion:
1% typical, 3% maximum
Squelch:
Adjustable 0.3 to 1.0 μV RF input, minimum

ENVIRONMENTAL

Shock:
Up to 10 g's in any direction
Vibration:
Up to 10 g's on any major axis
Temperature:
−30° to 60°C (−20° to 140°F), operating
−50° to 85°C (−60° to 185°F), storage
Humidity:
Up to 90% relative
Altitude:
Sea level to 20,000 feet

MECHANICAL

Housing: 5.00" x 2.95" x 1.25"
Single piece 2024-T3 aluminum alloy
Mounting:
Flanges on each end
Connectors:
RF — Type "N", options available
DC — Bendix PT02E-8-4P
(Mating connector provided)

THEORY OF OPERATION: R45F

RF Input Filter:

The RF Input Filter is of band-pass design and serves three basic functions: (1) It matches the receiver to a 50 ohm RF input, (2) It provides rejection of the image frequency, (3) It matches the RF input to the RF Amplifier.

RF Amplifier:

The RF Amplifier is designed for best gain vs. noise characteristics. It compensates for the loss of the RF Input Filter, and sets the noise figure for the receiver.

1st Local Oscillator:

The 1st L.O. is a Colpitts circuit which employs a high quality crystal and temperature compensating capacitors (TCXO) to maintain receiver frequency stability over the operating temperature range. The frequency of this crystal uniquely determines the received signal which will produce a 21.4MHz 1st I.F. For best stability, this oscillator is operated at one-ninth the injection frequency. Field frequency change may result in using a crystal with temperature characteristics which will not insure specified frequency stability over the temperature range, and is discouraged.

1st L.O. Frequency Triplers:

These stages multiply the frequency of the 1st L.O. for injection into the 1st Mixer at a frequency which is 21.4MHz below the desired signal. Double-tuned tank coils are employed to restore the spectral purity of the multiplied signal, and to reduce unwanted mixer products. Multiplying also provides a measure of isolation between TCXO and injection, which eliminates frequency "pulling" of the TCXO by subsequent tuning.

1st Mixer:

The First Mixer combines the RF input and the 1st L.O. injection signal to produce an I.F. of 21.4MHz. This 1st I.F. is then applied directly to the Selectivity Filter, FL1.

21.4MHz Selectivity Filter:

Receiver selectivity is primarily determined by the 8-pole, band-pass, crystal filter of tandem monolithic design employed at the first I.F. This filter insures optimum receiver performance in congested areas of the UHF band. Its output is buffered to prevent loading by subsequent stages.

FM Subsystem:

The basic "receiver" is contained within the Integrated Circuit U1. This I.C. contains the following circuit functions:

A. The 2nd Local Oscillator, whose frequency is determined by Y2.
B. Several stages of 2nd I.F. Amplification and Limiting at 455KHz.
C. Additional selectivity filtering at the 2nd I.F. (FL2).
D. Detection (Quadrature Coil L6).
E. Squelch circuitry.

Audio Amplifier:

Audio output from U1 must be amplified to meet specified levels. This is accomplished by Integrated Circuit U2, with the audio output level controlled by the potentiometer R18.

Audio Filter:

Amplifier audio output is passed through a 3-pole Butterworth active filter which attenuates all audio signals above 3KHz. This results in an improved signal-to-noise ratio at the receiver output. The output impedance of this filter is very low (approximately 1 ohm), allowing it to drive almost any load.

Voltage Regulator:

For stable receiver operation independent of varying input supply voltage--such as a discharging battery--a Voltage Regulator is employed to suppy all active stages. This regulator insures constant operation for supply voltages down to the specified minimum.

TUNING PROCEDURE: R45F

Step 1:
Apply 13.8VDC between Pin A of J2 and ground (Pin D), and connect a signal generator of known accuracy to the RF input connector. Adjust the RF Generator to the receiver frequency of operation, and adjust the FM to 5KHz deviation at 1KHz modulating frequency.

*Note 1: The Signal Generator must be precisely on frequency, otherwise distortion adjustments and S+N/N measurements may be meaningless. This is true for all NBFM receivers. A portable Signal Generator may have an internal oscillator that is less than 0.001% accurate, which could result in significant tuning error due to the highly selective I.F. filters and high-Q detector required for NBFM reception.

If the Signal Generator's operating characteristics are not known, do not attempt retuning!

Step 2:
Be sure the 1st Local Oscillator is precisely on frequency. This is best done by means of a pick-up loop of about 2 turns attached to a coax cable being held over the top of L11 (1st L.O. output tank coil), while observing the frequency on a Counter. (Again, the internal oscillator of the Counter must be on frequency to allow accurate tuneup. This means it must be within at least ±100Hz. Portable frequency counters are most often not within the limits!) Any necessary adjustment of 1st L.O. frequency is made by slightly adjusting the tuning slug of L7. If a totally different frequency within the specified band of operation is desired (eg. a different crystal on a new frequency), the retuning of L7 and re-peaking of L8, L9, L10 and L11 may be more pronounced.

*Note 2: If a new frequency of operation is required, the temperature drift characteristics of the new crystal must be known in addition to the accuracy of the test equipment.
All Monitron Transmitters and Receivers are temperature compensated to specified limits when originally manufactured or when returned for frequency change. A 1st L.O. crystal exhibiting excessive drift with temperature changes will cause less than specified receiver performance.

Step 3:
With the RF Signal Generator functioning in a known and accurate manner, and with the 1st L.O. on-frequency with its output peaked (eg. 1st Mixer input maximized), the recovered 1KHz audio output signal (Pin B) is observed with both an Oscilloscope and a Distortion Analyzer. The RF Signal Generator is adjusted to an RF output level of about - 80dbm, and the Receiver audio output is adjusted by means of

potentiometer, R18, to produce the desired level of output within the specified limits. Distortion is now measured, and is minimized by slightly "rocking" the slugs of L6 (Detector), and L4, and L5, (Filter matching) simultaneously, until a minimum reading is achieved. This should be 1% or less. Readings greater than 1% generally indicate test equipment inaccuracies.

*Note 3: The Squelch potentiometer, R19, must be fully CCW (defeated) when attempting receiver tuning.

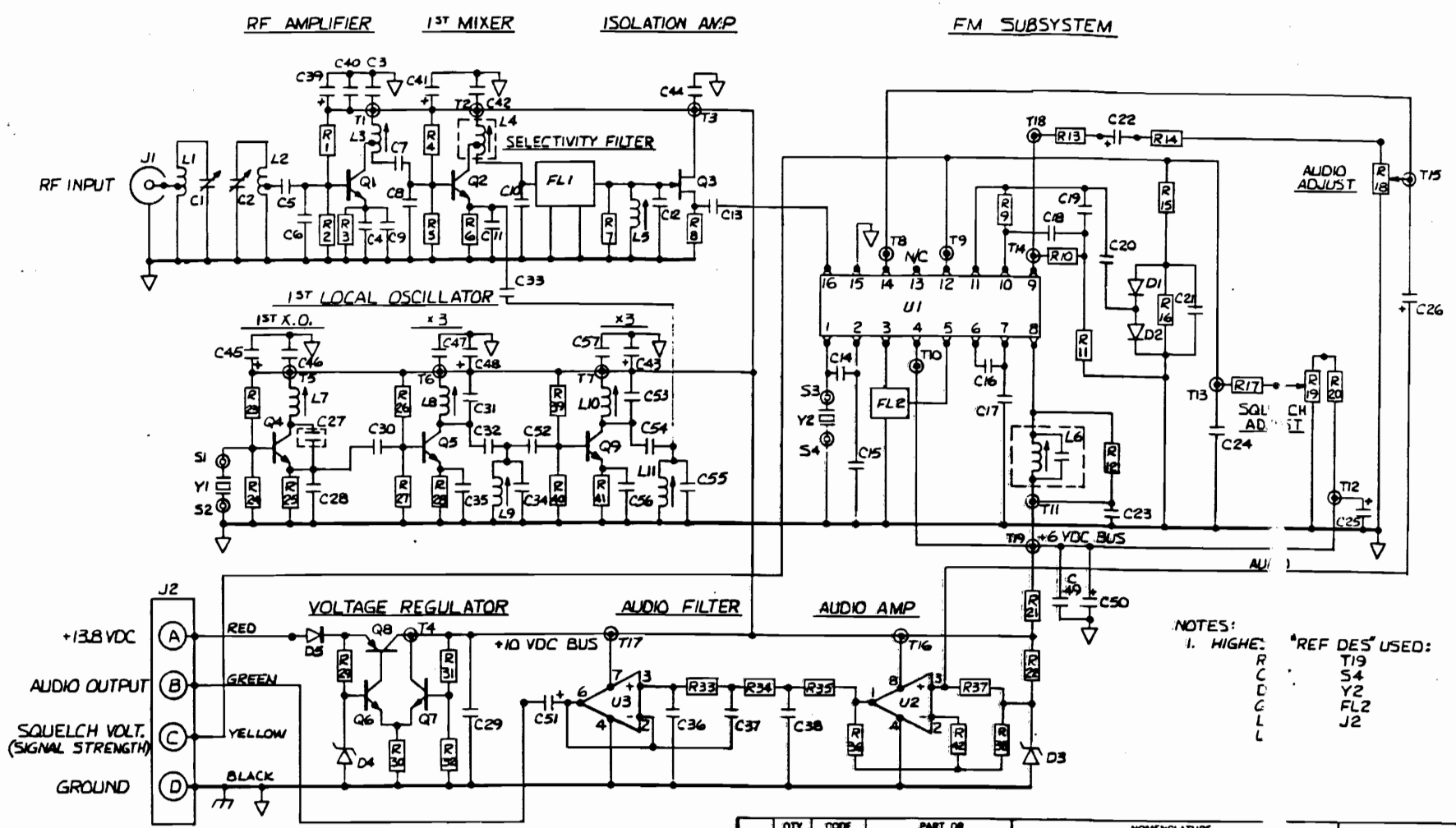
Step 4:
Reduce the RF Signal Generator output to 1 microvolt, leaving 1KHz Modulation and 5KHz Deviation settings as before. The recovered audio signal should be "noisy" and may show a slight decrease in audio output level. With the RF test signal maintained at 1 microvolt, kill the generator 1KHz modulation. The audio output voltage should drop over 20db, as indicated on an RMS voltmeter, leaving only the noise component in the receiver output. Retune L1, L2, and L3 to minimize this reading. Normally this requires only a slight repositioning of the tuning slugs, unless a new frequency at the opposite band extreme is selected. The ratio (in dB) of the audio output reading with 1KHz modulation to that without modulation is the receiver's S+N/N ratio, in dB, at 1 microvolt.

Step 5:
A recheck of the 1st L.O. tuning compensation may be necessary as the lid is placed on the unit ("lid effect"). Recheck the 1st L.O. frequency while covering L7 with the lid. Readjust as necessary for proper L.O. frequency with the lid over L7.

Step 6:
(1) Recheck audio output level for desired setting. (2) Reset Squelch potentiometer, R19, to desired RF "trip" level. This should never be above 1 microvolt, with 0.5 microvolt a good choice.

This completes the receiver tuning.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:
1. HIGHE

"REF DES" USED:

R	T19
C	S4
D	Y2
G	FL2
L	J2
U	

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

CONTRACT NO.

APPROVALS	DATE
DRAWN	12/18/85
CHECKED	12/18/85

MATERIAL

FINISH

NEXT ASSY	USED ON
	R45F
	R40F

MONITRON Corporation

SCHEMATIC - UHF RECEIVER (MODEL R45F)

SIZE	CODE IDENT NO	DRAWING NO
C		85C0057

SHEET 1 OF 1

PARTS LIST: R45F

Resistors: (All 1/4W, 5% carbon unless noted)

R1 = 20K
R2 = 10K
R3 = 2K
R4 = 20K
R5 = 4.7K
R6 = 2K
R7 = 3K
R8 = 2K
R9 = 390K
R10 = 20K
R11 = 750 OHM
R12 = 10K
R13 = 6.8K
R14 = 10K
R15 = 100K
R16 = 390K
R17 = 68K
R18 = 10K, Potentiometer
R19 = 50K, Potentiometer
R20 = 51K
R21 = 1K
R22 = 10K
R23 = 20K
R24 = 10K
R25 = 2K
R26 = 20K
R27 = 4.7K
R28 = 2K
R29 = 10K
R30 = 10K
R31 = 5.6K
R32 = 6.2K
R33 = 30K
R34 = 30K
R35 = 30K
R36 = 220K
R37 = 10K
R38 = 10K
R39 = 20K
R40 = 4.7K
R41 = 2K
R42 = 10K

Capacitors: (all pf values DM-5 silver mica unless noted)

C1 = .35-3.5pf, Johanson, 5802
C2 = .35-3.5pf, Johanson, 5802
C3 = .001mfd
C4 = .001mfd
C5 = 4pf
C6 = 8pf
C7 = 5pf
C8 = 10pf
C9 = .001mfd
C10 = 39pf
C11 = .01mfd
C12 = 18pf
C13 = .01mfd
C14 = 30pf
C15 = 120pf
C16 = .1mfd
C17 = .1mfd
C18 = .001mfd
C19 = .001mfd
C20 = .1mfd
C21 = .1mfd
C22 = 1.0mfd
C23 = .1mfd
C24 = .1mfd
C25 = 1.0mfd
C26 = 1.0mfd
C27 = 33N220 typical (sel)
C28 = 75pf
C29 = .01mfd
C30 = 10pf
C31 = 15pf
C32 = (sel)
C33 = 1pf
C34 = 15pf
C35 = .001mfd
C36 = 220pf, 2%
C37 = 3800pf, 2%
C38 = 1500pf, 2%
C39 = 1.0mfd
C40 = .001mfd
C41 = 1.0mfd
C42 = .001mfd
C43 = 1.0mfd
C44 = .01mfd
C45 = 1.0mfd
C46 = .001pf
C47 = .001mfd
C48 = 1.0mfd
C49 = .01mfd
C50 = 1.0mfd
C51 = 10mfd
C52 = 5pf
C53 = 3pf
C54 = (sel)
C55 = 3pf
C56 = .001mfd
C57 = .001mfd

PARTS LIST R45F

Q1 = MRF-904, Motorola
Q2 = MRF-904, Motorola
Q3 = 2N5485, Motorola
Q4 = 2N5222, Motorola
Q5 = 2N5222, Motorola
Q6 = 2N5223, Motorola
Q7 = 2N5223, Motorola
Q8 = 2N5226, Motorola
Q9 = 2N5222, Motorola

U1 = LM3361AN, National
U2 = TL062CP, TI
U3 = TL061CP, TI

D1 = 1N4148
D2 = 1N4148
D3 = LVA-51A, TRW
D4 = LVA-51A, TRW
D5 = 1N4001

Inductors:

L1 = 2 3/4T, #20, .26"I.D., 1/4" long. Tap @ 1/2 turn
L2 = 3T, #20, .26"I.D., 1/4" long. Tap @ 3/4 turn
L3 = 1 3/4T, #26, Tap at mid-point
L4 = 15 1/2T, #32, Tap at 9 3/4 turn
L5 = 22 1/2T, #32
L6 = Purchaed Assembly, RMC-286597HM, Toko America
L7 = 9 1/4T, #26
L8 = 3 1/4T, #26
L9 = 3 1/4T, #26
L10 = 1 3/4T, #26
L11 = 1 3/4T, #26

Miscellaneous:

FL1 = 21.4MHz Filter, 1631, PTI
F12 = 455 KHz Filter, CFU-455, MURATA

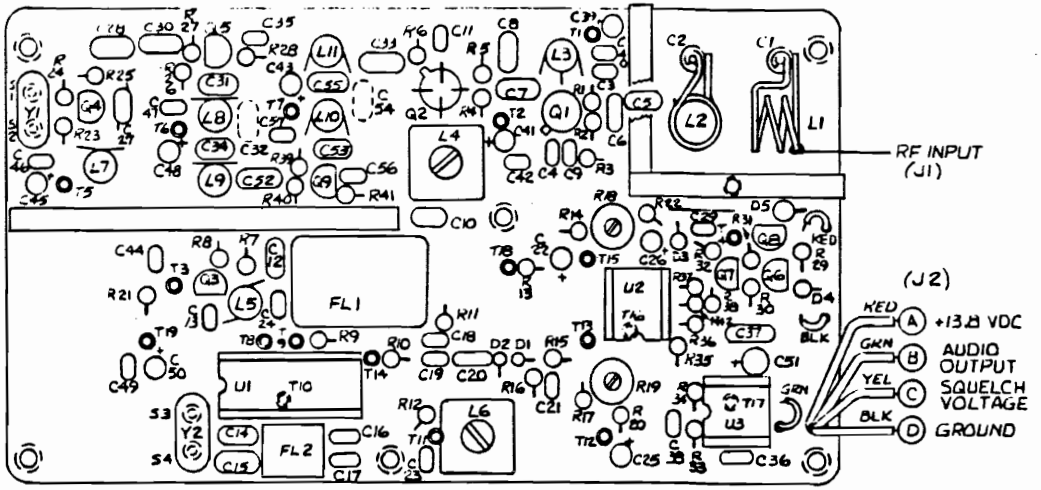
Y1 = Crystal, 3rd O.T., Series, F = $\left(\frac{F_{rec} - 21.4MHz}{9}\right)MHz$
Y2 = Crystal, Fundamental, 20.94MHz, 32pf

T1 - T19 = Terminal, 160-2041-02-01-0, CTC

S1 - S4 = Socket, 450-3704-01-06, CTC

J1 = Connector, RF, UG-58A/U, (Type "N")
J2 = Connector, D.C., PT02E-8-4P, Bendix

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE.
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN [illegible]	1/9/96
CHECKED	

MONITRON Corporation

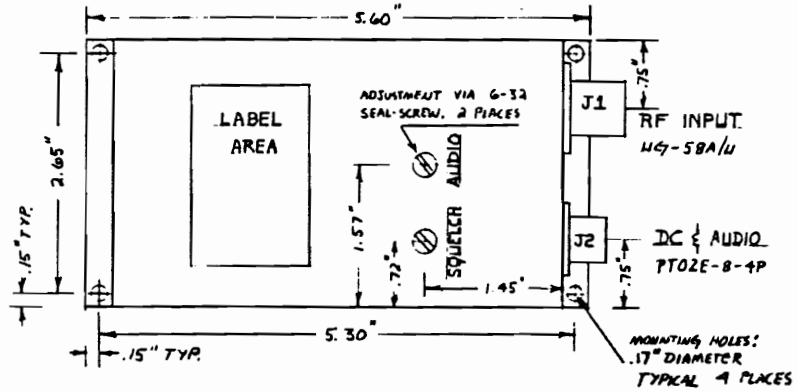
PWB ASSEMBLY-
RECEIVER, UHF
R45F

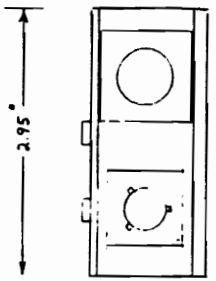
SIZE	CODE IDENT NO	DRAWING NO
C		94C0038

SCALE [illegible] SHEET OF

93C0019	R45F
NEXT ASSY	USED ON
APPLICATION	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



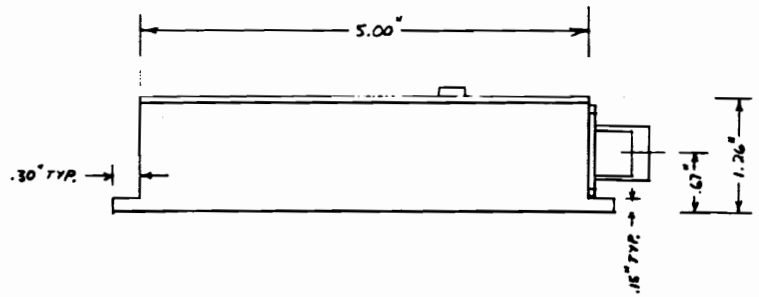


NOTES:

1. RECOMMENDED ADJUSTMENT TOOL: JOHANSON 8766

PIN CONNECTIONS:

A. +12 VDC.
B. AUDIO OUTPUT
C. SIGNAL STRENGTH
D. AUDIO & POWER RETURN



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

CONTRACT NO

APPROVALS	DATE
DRAWN MLM	8-30-77
CHECKED	

MATERIAL: AL. ALLOY 2024-T3

FINISH: IRRADITE / KRYLON

R45F
TR-2

NEXT ASSY | USED ON

MONITRON Corporation

OUTLINE R45F
UHF RECEIVER

SIZE	CODE IDENT NO	DRAWING NO
C		7740C02

WARRANTY AND COMPANY POLICY:

Monitron Corporation warrants the above equipment against all material or manufacturing defects for a period of one year from the date of purchase. This warranty does not cover extraordinary instances resulting in damage to the equipment.

Monitron is constantly striving to improve its radio product line; for this reason, all published specifications, schematic diagrams, or other technical information relative to these products are subject to change without notice.

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Bæklingur um sendi

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

INSTRUCTION MANUAL

UHF NBFM TRANSMITTER

MODEL T45F-1

MODEL T45F-2

(400-475MHz)

June 1986

Monitron Corporation
P.O. Box 27485
Tulsa, Oklahoma 74149-0485
(918) 836-6831)

87108 MODEL T 45 F -1 S/N 1251

FINAL TEST DATA

Test Item:	+25°C	-30°C	+60°C
E_{in} (VDC)	13.8	13.8	13.8
I_{in} (ma)	88	84	86
P_{out} (mw)	195	225	165
f_{out} (MHz)	469.500	469.5015	469,5000
Dev. Sens. (KHz/VRMS)	5.0/1.0	5.0/1.0	5.0/1.0
Audio Limiting (VRMS)	1.0	1.0	1.0

Voltage Regulator: 8.71 VDC.

Spectral purity: $2f_o$ = -55 dbc.

VSWR: ∞ Voh

Distortion: @ 1KHz @ 2/3 deviation 0.3 %.

Final acceptance: MBH

Date: 12-21-87

Notes:

Pin Connections:

A = +13.8 VDC Brown
B = Modulation Input Blue
C = ~~Ground~~
D = Ground from Gulw

INDEX

TRANSMITTER

GENERAL DESCRIPTION:

The Monitron Model T45F is an all solid-state, narrowband, FM transmitter designed to provide superior transmission of signals in the 400-475MHz UHF band. It is available as a low-power T45F-1, or a higher-power T45F-2.

In addition to its low power consumption and excellent spectral purity, every effort has been made to maintain very low distortion of the modulating signal, along with an essentially flat frequency response over the modulation bandwidth. These qualities are maintained throughout the operating temperature range.

Only quality components are used in the manufacture of the transmitter; these are mounted on a single-sided printed circuit board. Most components are visible upon removal of the cover and all parts are readily accessible for test or replacement.

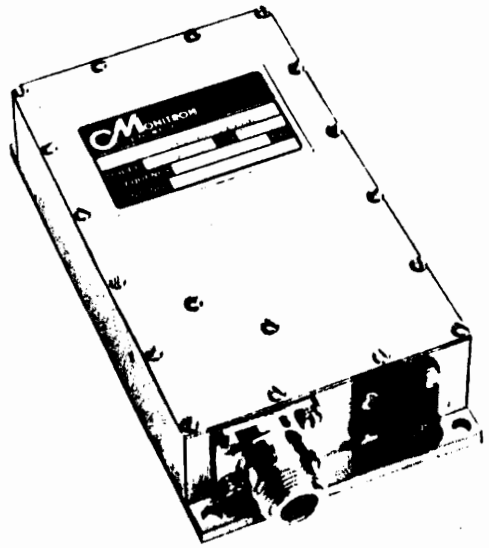
The transmitter is housed in a thick-walled aluminum alloy box, machined from a single piece of bar stock. This results in a seamless, almost indestructible housing which is RF "tight" and impervious to the environment.

These salient features--technical excellence, quality of manufacture, reliability and durability--make these transmitters ideal for those engaged in telemetering scientific data.

Monitron also manufactures a series of NBFM UHF receivers designed as companion units for the above transmitters, as well as a complete line of VHF equipment.

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

UHF TELEMETRY TRANSMITTER



MODEL T45F-1

- **NBFM — ANALOG OR DIGITAL DATA**
- **HIGH RELIABILITY — 100% TESTED**
- **MILITARY QUALITY — EXTREMELY RUGGED**
- **HIGH EFFICIENCY**
- **RF OUTPUT POWER TO 400mW**
- **1 YEAR WARRANTY**

SPECIFICATIONS — MODEL T45F-1

GENERAL

Transmitter Type:
Frequency Modulation (Narrow Band FM)
Frequency Range:
400 to 475 MHz.
Factory preset to any single frequency within this band (Other frequencies available).

ELECTRICAL

Input Power:
11 to 15 Vdc @ 80 mA typical for 150 mw RF output power
Power Protection:
Protected against reversed supply polarity;
Internally regulated
Output Power:
Factory preset, 100-400mW (specify power with order)
Frequency Stability:
± 0.0005% of assigned frequency
Spurious Outputs:
Maximum level, 43 + 10 log (output power) dB below carrier
Output Impedance:
50 ohms
Load Protection:
Infinite VSWR withstood without damage.
Modulation Type:
16F3; ± 5 kHz for 100% @ 1 kHz modulation
Modulation Bandwidth:
300 to 3000 Hz, minimum
Modulation Response:
± 0.5 dB typical referred to 1 kHz; ± 1.5 dB maximum
Modulation Limiting:
Factory preset for 5 kHz deviation maximum
Modulation Distortion:
0.5% typical @ 1 kHz @ 2/3 deviation; 2% maximum
Deviation Sensitivity:
Factory preset for 5 kHz deviation with 1.0 V RMS modulation
Audio Input Impedance:
100 kilohms ± 10%

ENVIRONMENTAL

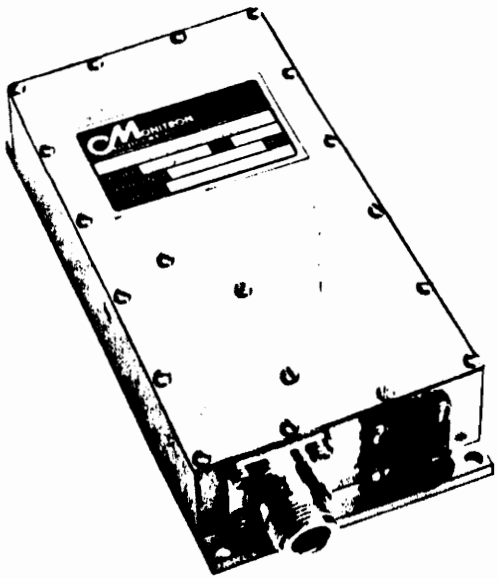
Shock:
Up to 10 g's in any direction
Vibration:
Up to 10 g's on any major axis
Temperature:
−30° to 60°C (−20° to 140°F), operating
−50° to 85°C (−60° to 185°F), storage
Humidity:
Up to 90% relative
Altitude:
Sea level to 20,000 feet

MECHANICAL

Housing:
4.50" x 2.75" x 1.25"
Single piece 2024-T3 aluminum alloy
Mounting:
Flanges on each end
Connectors:
RF — Type "N", options available
DC — Bendix PT02E-8-4P
(Mating connector provided)

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

UHF TELEMETRY TRANSMITTER



MODEL T45F-2

- **NBFM — ANALOG OR DIGITAL DATA**
- **HIGH RELIABILITY — 100% TESTED**
- **MILITARY QUALITY — EXTREMELY RUGGED**
- **HIGH EFFICIENCY**
- **RF OUTPUT 500mW TO 3 WATTS**
- **1 YEAR WARRANTY**

SPECIFICATIONS — MODEL T45F-2

GENERAL

Transmitter Type:
Frequency Modulation (Narrow-Band FM)
Frequency Range:
400 to 475 MHz
Factory preset to any single frequency within this band
(Other frequencies available).

ELECTRICAL

Input Power:
11 to 15 Vdc @ 300 mA typical for 1 Watt RF output power.
Power Protection:
Protected against reversed supply polarity; Power internally regulated
Output Power:
500 mW to 3 Watts; Factory preset
Frequency Stability:
± 0.0005% of assigned frequency
Spurious Signals:
Maximum level, 43 + 10 log (output power) dB below carrier
Output Impedance:
50 ohms
Load Protection:
Infinite VSWR withstood without damage. Adequate heat-sink required
Modulation Type:
16F3; ± 5 kHz for 100% @ 1 kHz modulation
Modulation Bandwidth:
300 to 3000 Hz, minimum
Modulation Response:
± 0.5 dB typical referred to 1 kHz; ± 1.5 dB maximum
Modulation Limiting:
Factory preset for 5 kHz deviation maximum
Modulation Distortion:
0.5% typical @ 1 kHz @ 2/3 deviation; 2% maximum
Deviation Sensitivity:
Factory preset for 5 kHz deviation with 1.0 V RMS modulation
Audio Input Impedance:
100 ohms ± 10%

ENVIRONMENTAL

Shock:
Up to 10 g's in any direction
Vibration:
Up to 10 g's on any major axis
Temperature:
-30° to 60°C (-20° to 140°F), operating
-50° to 85°C (-60° to 185°F), storage
Humidity:
Up to 90% relative
Altitude:
Sea level to 20,000 feet

MECHANICAL

Housing:
5.00" x 2.75" x 1.25"
Single piece 2024-T3 aluminum alloy
Mounting:
Flanges on each end
Connectors:
RF - Type "N"; options available
DC - Bendix PT02E-8-4P
(Mating connector provided)

THEORY OF OPERATION:

Temperature Compensated Crystal Oscillator (TCXO):

The carrier is generated at 1/36 the output frequency by a temperature compensated crystal oscillator, or TCXO. The combination of a quality fundamental-mode crystal and circuit temperature compensation results in an oscillator that readily satisfies the FCC requirement of ±0.0005% frequency stability over the specified operating temperature range.

Buffer:

To insure that the precision TCXO is isolated from the effects of subsequent stages, an emitter-follower Buffer stage is connected to the output of the TCXO. This allows carrier modulation or tuning of subsequent stages without frequency "pulling".

Modulator:

The Modulator is actually a phase-modulator preceded by a 6db/octave de-emphasis network, R46 and C54. This network counteracts the 6db/octave pre-emphasis characteristic of PM and produces a resultant FM response over the specified modulation bandwidth.

Because of the high modulation index required for full-rated deviation at 300Hz modulating frequency, a cascade phase-modulator using parallel, variable-capacitance diodes is used to achieve this result while maintaining very low modulation distortion.

Frequency Multipliers:

All Frequency Multiplier stages can be described as having the same basic functions of multiplying and amplifying their respective input signals. Double-tuned output circuits are employed to retain spectral purity during the multiplication process. The output of the Multiplier chain is approximately 25mw at the desired output frequency.

Driver:

The Driver stage amplifies the signal from the Frequency Multiplier chain to the specified output level. To obtain best DC to RF conversion efficiency, this stage is supplied directly from the unregulated voltage bus. The RF output power therefore "follows" the supply voltage, showing approximately a 2db change as the supply changes from 12 to 15VDC. This stage can be supplied from the Voltage Regulator if an unchanging RF output is desired.

Power Amplifier:

The T45F-2 has an additional stage of power amplification for those applications requiring higher RF output power. Gain of this stage is approximately 9db. This stage may also be supplied from the Voltage Regulator if unchanging RF output is desired.

Data Amplifier, Limiter, Buffer:

A variable-gain amplifier stage, U1, preceding the Limiter, allows any data level between 0.1 and 1.0VRMS to produce full-rated deviation of the transmitter. Once this level is selected, the gain of U1 is adjusted, by means of R41, until "clipping" of the data signal just occurs. This can be seen with an oscilloscope at pin 4 or pin 10 of U1, and can be most easily set using a sine-wave data signal of approximately 300Hz.

Once this clipping level has been set, any data signal of greater amplitude will be symmetrically clipped by the Limiter stage. The Limiter output is buffered to prevent loss of limiting symmetry due to loading.

Modulation Filter:

Clipping of the data signal produces harmonics which, if unattended, could produce unwanted modulation sidebands. By following the Limiter with a low-pass Modulation Filter, all frequency components above 3KHz are attenuated more than 12db/octave as required by EIA Standard RS-152-B

Voltage Regulator:

For stable transmitter operation independent of input supply voltage--such as a discharging batery--a Voltage Regulator is employed to supply all stages. This regulator insures constant operation for supply voltages down to the specified minimum.

TUNING PROCEDURE:

Step 1, RF Output Power and Frequency:

Connect a wattmeter with 50 ohm load and a frequency counter to the RF output connector, J1, through a coupling device, such as a Directional Coupler, as a means of providing a sample output signal simultaneously with RF power measurement. The coupling coefficient should be at least -20db. The wattmeter should have a full-scale range consistent with the transmitter output power. Connect DC power to J2, but do not apply modulation at this time.

Starting with the first Multiplier stage, slightly tune the double-tuned tank coils while observing a change in supply current. Tune for peak current. Repeat through all Multiplier stages.

Tuning of the Driver and Power Amplifier stages consists of adjusting the trimmer capacitors associated with these stages. Any adjustment should produce a noticable input current change and corresponding output power change. Adjust each trimmer for maximum RF output power. (One exception is C42, which together with L19 form a series resonant trap at the second harmonic of the RF output on the Model T45F-2. Do not adjust C42 without some means of measuring the second harmonic, such as a spectrum analyzer.)

Should it be necessary to reset the RF output frequency, this may be done by adjusting the trimmer capacitor which is in parallel with the crystal. Retouch all tuning adjustments while observing RF output power and frequency. Tune for peak RF output.

The above tuning procedure is minimal in that it allows no means of measuring spurious and harmonic signals present at the RF output. It is recommended that any retuning be done while utilizing a spectrum analyzer connected to the coupling port mentioned above. The above procedure is then expanded to tuning simultaneously for maximum RF output power with minimum spurious content. C42 may also then be set for maximum rejection of the second harmonic, as viewed on the spectrum analyzer.

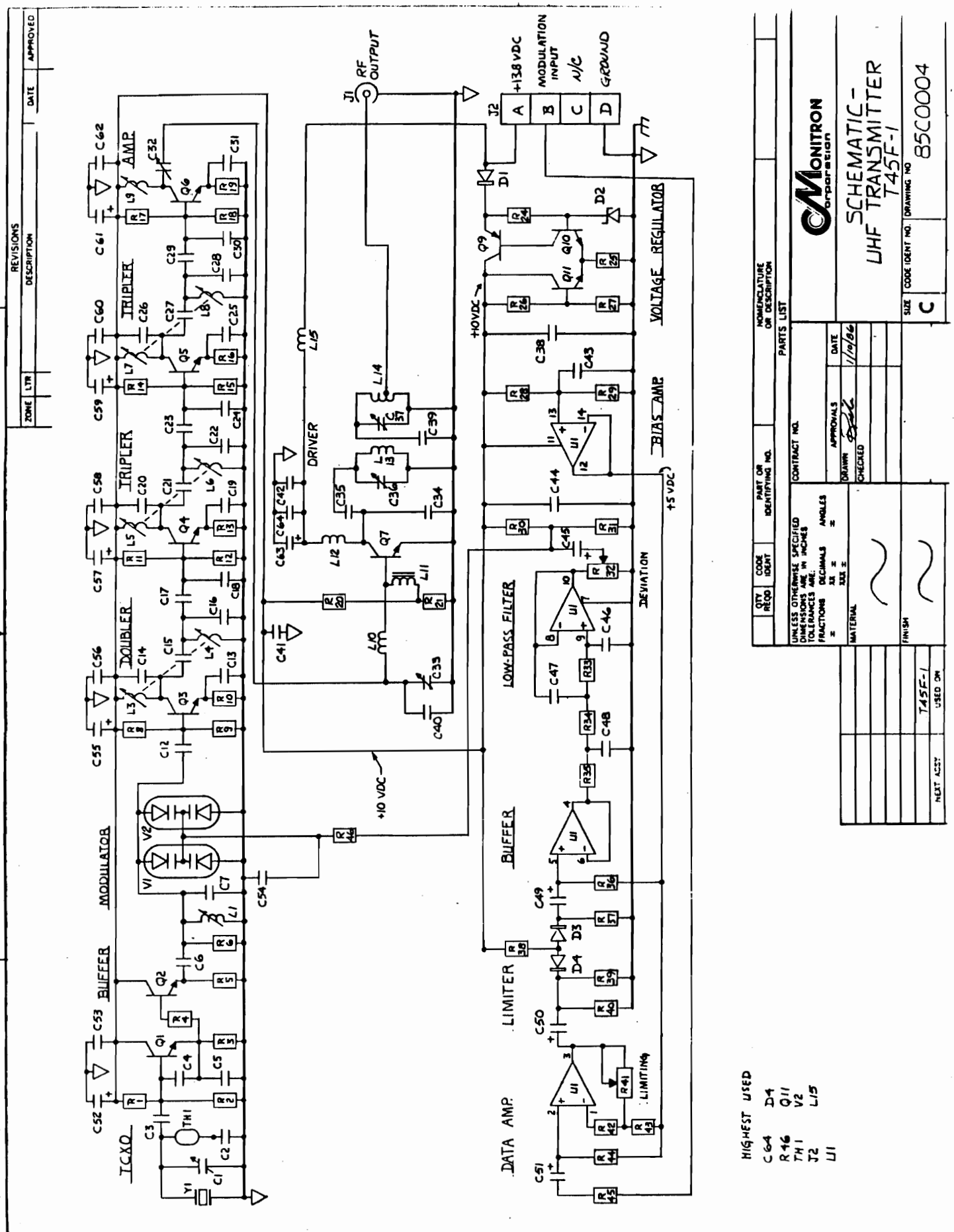
Step 2, Modulation Characteristics:

Apply modulation. Adjust the modulation frequency to 2.078KHz at 1.0VRMS. (Unless otherwise specified, 1.0VRMS modulation will produce 5.0KHz deviation.) Spectrum analysis of the RF output--by means of the isolated port on the Directional Coupler--should show the first carrier null, indicating 5.0KHz of deviation. If not, adjust the Deviation Sensitivity control accordingly.

The modulating signal level at which limiting occurs can be checked by increasing the modulation amplitude until spectral analysis shows higher order modulation sidebands being produced. The limiting level should always be set above the highest deviation required, to prevent

signal distortion (clipping) of normal modulation signals. If limiting is already imposed on the modulating signal, then limiting within the transmitter is redundant and should be adjusted such as to not introduce any distortion at maximum deviation.

With the transmitter on frequency and tuned for RF power and the modulation input level established, the only remaining tuning check is that of the Modulator. Set the audio signal generator frequency to 1KHz and reduce the modulation amplitude to produce 2/3 rated deviation. With the recovered audio applied to a Distortion Meter, slightly adjust the modulator coil , L1, while observing the distortion reading. It should abruptly dip to a reading of less than 1%. Readjust the Deviation potentiometer, R32, if necessary, to re-establish 5.0KHz of deviation with 1.0VRMS modulation amplitude.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SCHEMATIC - UHF TRANSMITTER T45F-1
MONITRON Corporation
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CHECKED
DATE 11/10/86
SIZE C
CODE IDENT NO.
DRAWING NO 85C0004
T45F-1
NEXT ASSY
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FINISH
MATERIAL
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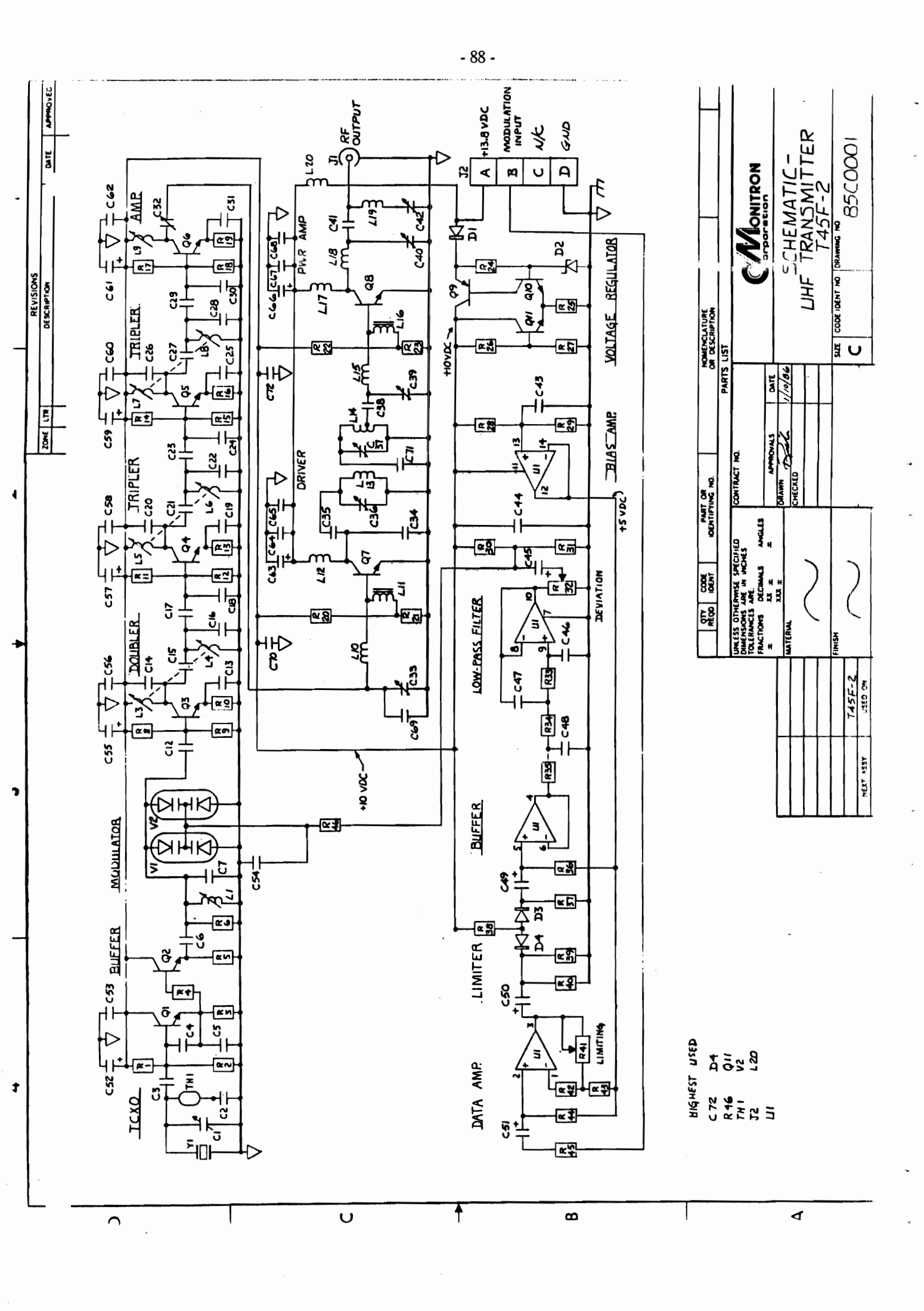
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
ICXO
BUFFER
MODULATOR
DOUBLER
TRIPLER
TRIPLER
AMP
DRIVER
RF OUTPUT
+13.8 VDC
MODULATION INPUT
A/C
GROUND
VOLTAGE REGULATOR
BIAS AMP
+5 VDC
+10 VDC
DEVIATION
LOW-PASS FILTER
BUFFER
LIMITER
DATA AMP.
LIMITING
HIGHEST USED
C64 D4
R46 Q11
TH1 V2
J2 L15
U1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TRIPLER
AMP
DOUBLER
MODULATOR
BUFFER
IOXO
DRIVER
PWR AMP
LOW-PASS FILTER
BUFFER
LIMITER
DATA AMP
BIAS AMP
VOLTAGE REGULATOR
DEVIATION
LIMITING
RF OUTPUT
+13.8 VDC
MODULATION INPUT
N/C
GND
+10 VDC
+5 VDC
+HOVDC
HIGHEST USED
C72 D4
R46 Q11
TH1 V2
J2 L20
U1
PARTS LIST
NOMENCLATURE OR DESCRIPTION
PART OR IDENTIFYING NO.
CODE IDENT
QTY REQD
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES
CONTRACT NO.
APPROVALS
DRAWN
CHECKED
DATE
11/10/86
MATERIAL
FINISH
T45F-2
NEXT ASSY
USED ON
MONITRON corporation
SCHEMATIC - UHF TRANSMITTER T45F-2
SIZE
C
CODE IDENT NO
DRAWING NO
85C0001

T45F-1

PARTS LIST:

Resistors: (All 1/4W, 5% carbon unless noted)

R1 = 20K
R2 = 10K
R3 = 2K
R4 = 1K
R5 = 1K
R6 = 10K
R7 = Not used
R8 = 10K
R9 = 3.9K
R10 = 1K
R11 = 10K
R12 = 3.9K
R13 = 1K
R14 = 10K
R15 = 3.9K
R16 = 1K
R17 = 10K
R18 = 3.9K
R19 = (sel) 1K Typ.
R20 = 2K
R21 = 100 OHMS
R22 = Not used
R23 = Not used
R24 = 5.6K
R25 = 2K
R26 = 5.6K
R27 = 6.2K
R28 = 100K
R29 = 100K
R30 = 100K
R31 = 39K
R32 = 10K Potentiometer
R33 = 30K
R34 = 30K
R35 = 30K
R36 = 100K
R37 = 10K
R38 = 20K
R39 = 10K
R40 = 20K
R41 = 100K Potentiometer
R42 = 10K
R43 = 1K
R44 = 10K
R45 = 100K
R46 = 100K

Capacitors: (All pf values DM-5 silver mica unless noted)

C1 = 1.7-6pf NPO Trimmer
C2 = 5pf
C3 = (sel) 33N750 Typ.
C4 = 100pf
C5 = 100pf
C6 = 5pf
C7 = 56N450
C8 = Not used
C9 = Not used
C10 = Not used
C11 = Not used
C12 = 10pf
C13 = .01mfd
C14 = 33pf
C15 = 1pf
C16 = 33pf
C17 = 10pf
C18 = 47pf
C19 = .001mfd
C20 = 20pf
C21 = (sel)
C22 = 20pf
C23 = 5pf
C24 = 10pf
C25 = .001mfd
C26 = 10pf
C27 = .1pf Molded
C28 = 10pf
C29 = 3pf
C30 = (sel)
C31 = .001mfd
C32 = .35-3.5pf Trimmer
C33 = 1-14pf Trimmer
C34 = 2pf
C35 = 3pf
C36 = .35-3.5pf Trimmer
C37 = .35-3.5pf Trimmer
C38 = .001mfd
C39 = 1pf
C40 = 10pf
C41 = .001mfd
C42 = 10pf
C43 = .001mfd
C44 = .01mfd
C45 = 1.0mfd
C46 = 220pf, 2%
C47 = 3800pf, 2%
C48 = 1500pf, 2%
C49 = 1.0mfd
C50 = 1.0mfd
C51 = 1.0mfd
C52 = 1.0mfd
C53 = .01mfd
C54 = .015mfd, Mylar
C55 = 1.0mfd
C56 = .01mfd
C57 = .001mfd
C58 = 1.0mfd
C59 = 1.0mfd
C60 = .001mfd
C61 = 1.0mfd
C62 = .001mfd
C63 = 1.0mfd
C64 = .001mfd

T45F-1

PARTS LIST:

Semiconductors:

Q1 = 2N5222, Motorola
Q2 = 2N5222, Motorola
Q3 = 2N5222, Motorola
Q4 = 2N5222, Motorola
Q5 = 2N5222, Motorola
Q6 = MPSH10, Motorola
Q7 = 2N4429, Motorola
Q8 = Not used
Q9 = 2N4919, Motorola
Q10 = 2N5223, Motorola
Q11 = 2N5223, Motorola
U1 = RC4136DB Ray.
V1 = MV104, Motorola
V2 = MV104, Motorola
D1 = IN4001, Motorola
D2 = LVA-51A, TRW
D3 = 5082-2912, H.P.
D4 = 5082-2912, H.P.

Inductors:

L1 = 14 3/4T #32
L2 = Not used
L3 = 14 3/4T #32
L4 = 14 3/4T #32
L5 = 5 1/4T #26
L6 = 5 1/4T #26
L7 = 2 1/4T #26
L8 = 2 1/4T #26
L9 = 1 3/4T #22
L10 = 1/2T, Q7 Lead
L11 = 2T #32, Ferrite Bead
L12 = .22 microhenry molded choke
L13 = 2T #20, 1/4" I.D.
L14 = 2T #20, 1/4" I.D.
L15 = .27 microhenry molded choke

Miscellaneous:

Crystal = Fundamental Mode, Parallel Resonant,
32pf Load, HC-25/U Holder, I.C.M. #434575

$$\text{Crystal Freq.} = \frac{\text{Output Freq.}}{36} \text{ MHz.}$$

TH1 = 100 OHM @ 23°C
J1 = Connector, RF, UG-58A/U
J2 = Connector, DC, PT02E-8-4P, Bendix

T45F-2

PARTS LIST:

Resistors: (All 1/4W, 5% carbon unless noted)

R1 = 20K
R2 = 10K
R3 = 2K
R4 = 1K
R5 = 1K
R6 = 10K
R7 = Not used
R8 = 10K
R9 = 3.9K
R10 = 1K
R11 = 10K
R12 = 3.9K
R13 = 1K
R14 = 10K
R15 = 3.9K
R16 = 1K
R17 = 10K
R18 = 3.9K
R19 = (sel) 270 OHMS Typ.
R20 = 2K
R21 = 100 OHMS
R22 = 2K
R23 = 100 OHMS
R24 = 5.6K
R25 = 510 OHMS
R26 = 5.6K
R27 = 6.2K
R28 = 100K
R29 = 100K
R30 = 100K
R31 = 39K
R32 = 10K Potentiometer
R33 = 30K
R34 = 30K
R35 = 30K
R36 = 100K
R37 = 10K
R38 = 20K
R39 = 10K
R40 = 20K
R41 = 100K Potentiometer
R42 = 10K
R43 = 1K
R44 = 10K
R45 = 100K
R46 = 100K

Capacitors: (All pf values DM-5 silver mica unless noted)

C1 = 1.7-6pf NPO Trimmer
C2 = 5pf
C3 = (sel) 33N750 Typ.
C4 = 100pf
C5 = 100pf
C6 = 5pf
C7 = (sel)
C8 = Not used
C9 = Not used
C10 = Not used
C11 = Not used
C12 = 10pf
C13 = .01mfd
C14 = 33pf
C15 = 1pf
C16 = 33pf
C17 = 10pf
C18 = 47pf
C19 = .001mfd
C20 = 24pf
C21 = (sel)
C22 = 20pf
C23 = 5pf
C24 = 10pf
C25 = .001mfd
C26 = 10pf
C27 = .1pf Molded
C28 = 10pf
C29 = 3pf
C30 = (sel)
C31 = .001mfd
C32 = .35-3.5pf Trimmer
C33 = 1-14pf Trimmer
C34 = 2pf
C35 = 3pf
C36 = .35-3.5pf Trimmer
C37 = .35-3.5pf Trimmer
C38 = 3pf
C39 = 1-14pf Trimmer
C40 = .6-6pf Trimmer
C41 = 3pf, DM10
C42 = .35-3.5pf Trimmer
C43 = .001mfd
C44 = .01mfd
C45 = 1.0mfd
C46 = 220pf, 2%
C47 = 3800pf, 2%
C48 = 1500pf, 2%
C49 = 1.0mfd
C50 = 1.0mfd
C51 = 1.0mfd
C52 = 1.0mfd
C53 = .01mfd
C54 = .015mfd, Mylar
C55 = 1.0mfd
C56 = .01mfd
C57 = .001mfd
C58 = 1.0mfd
C59 = 1.0mfd
C60 = .001mfd
C61 = 1.0mfd
C62 = .001mfd
C63 = 1.0mfd
C64 = .001mfd
C65 = 10pf
C66 = 1.0mfd
C67 = .001mfd
C68 = 10pf
C69 = 10pf
C70 = .001mfd
C71 = 1pf
C72 = .001mfd

T45F-2

PARTS LIST:

Semiconductors:

Q1 = 2N5222, Motorola
Q2 = 2N5222, Motorola
Q3 = 2N5222, Motorola
Q4 = 2N5222, Motorola
Q5 = 2N5222, Motorola
Q6 = MPSH10, Motorola
Q7 = 2N4429, Motorola
Q8 = C3-12, C.T.C.
Q9 = 2N4919, Motorola
Q10 = 2N5223, Motorola
Q11 = 2N5223, Motorola
U1 = RC4136DB Ray.
V1 = MV104, Motorola
V2 = MV104, Motorola
D1 = IN4001, Motorola
D2 = LVA-51A, TRW
D3 = 5082-2912, H.P.
D4 = 5082-2912, H.P.

Inductors:

L1 = 14 3/4T #32
L2 = Not used
L3 = 14 3/4T #32
L4 = 14 3/4T #32
L5 = 5 1/4T #26
L6 = 5 1/4T #26
L7 = 2 1/4T #26
L8 = 2 1/4T #26
L9 = 1 3/4T #22
L10 = 1/2T, Q7 Lead
L11 = 2T #32, Ferrite Bead
L12 = .22 microhenry molded choke
L13 = 2T #20, 1/4" I.D.
L14 = 2T #20, 1/4" I.D.
L15 = 1T #20, 1/8" I.D.
L16 = 2T #32, Ferrite Bead
L17 = .22 microhenry molded choke
L18 = 1 1/2T #20, 1/4" I.D.
L19 = 2T #20, 1/8" I.D.
L20 = .27 microhenry molded choke

Miscellaneous:

Crystal = Fundamental Mode, Parallel Resonant, 32pf Load, HC-25/U Holder, I.C.M. #434575

$$\text{Crystal Freq.} = \frac{\text{Output Freq.}}{36} \text{ MHz.}$$

TH1 = 100 OHM @ 23°C
J1 = Connector, RF, UG-58A/U
J2 = Connector, DC, PT02E-8-4P, Bendix

REVISIONS				
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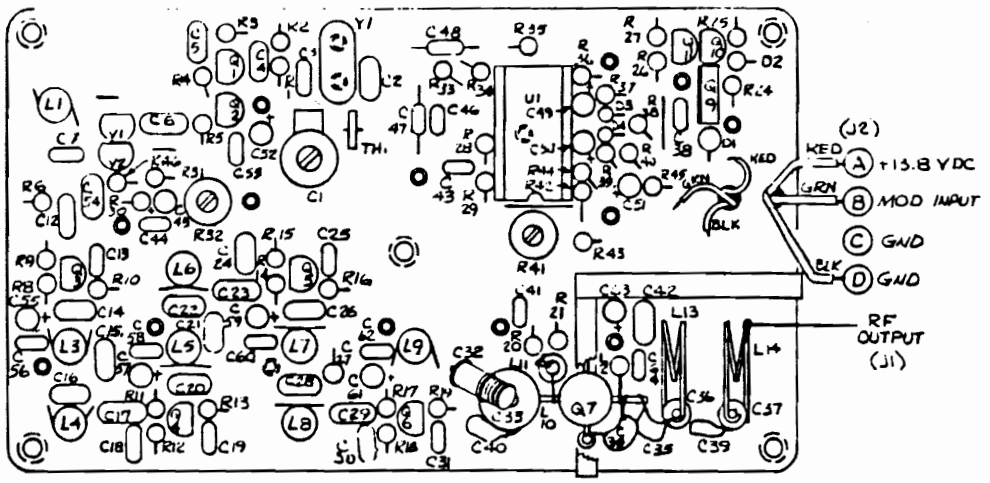

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PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

13C0004	T45F-1
NEXT ASSY	USED ON

APPLICATION

CONTRACT NO

APPROVALS	DATE
DRAWN	1/7/86
CHECKED	

MONITRON Corporation

PWB ASSEMBLY-
TRANSMITTER, UHF LOW PWR
T45F-1

SIZE	CODE IDENT NO	DRAWING NO
C		94C0004

SCALE — SHEET

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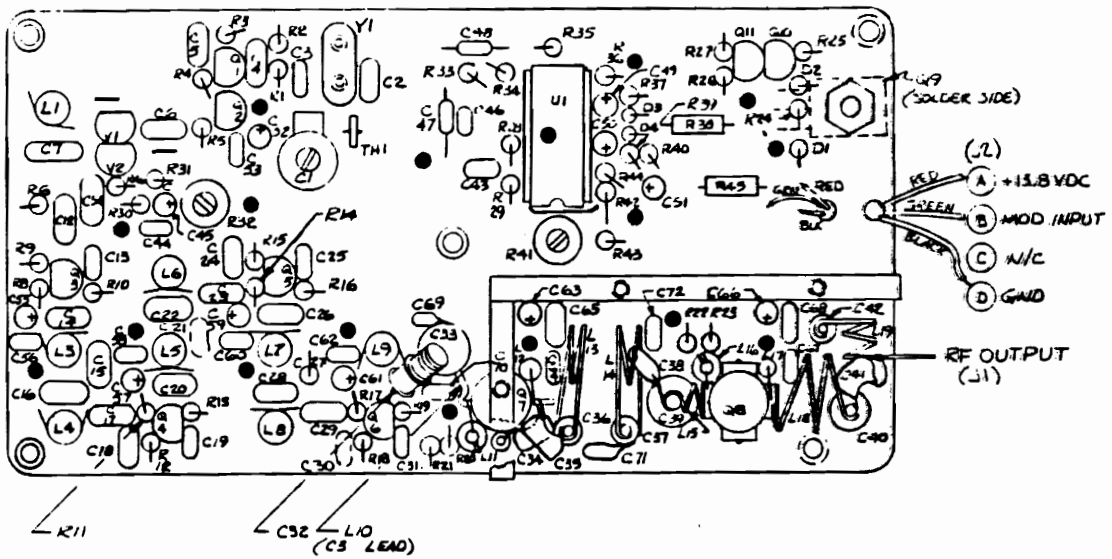

TYP ORIENTATION
FOR: D1,2,3,4

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL ~

FINISH ~

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	

MONITRON Corporation

PWB ASSEMBLY - TRANSMITTER, UHF, HIGH PWR
T45F-2

SIZE	CODE IDENT NO	DRAWING NO
C		74C0001

SCALE 2/1 SHEET 1 OF 1

93C0001	T45F-2
NEXT ASSY	USED ON
APPLICATION	

REVISIONS				
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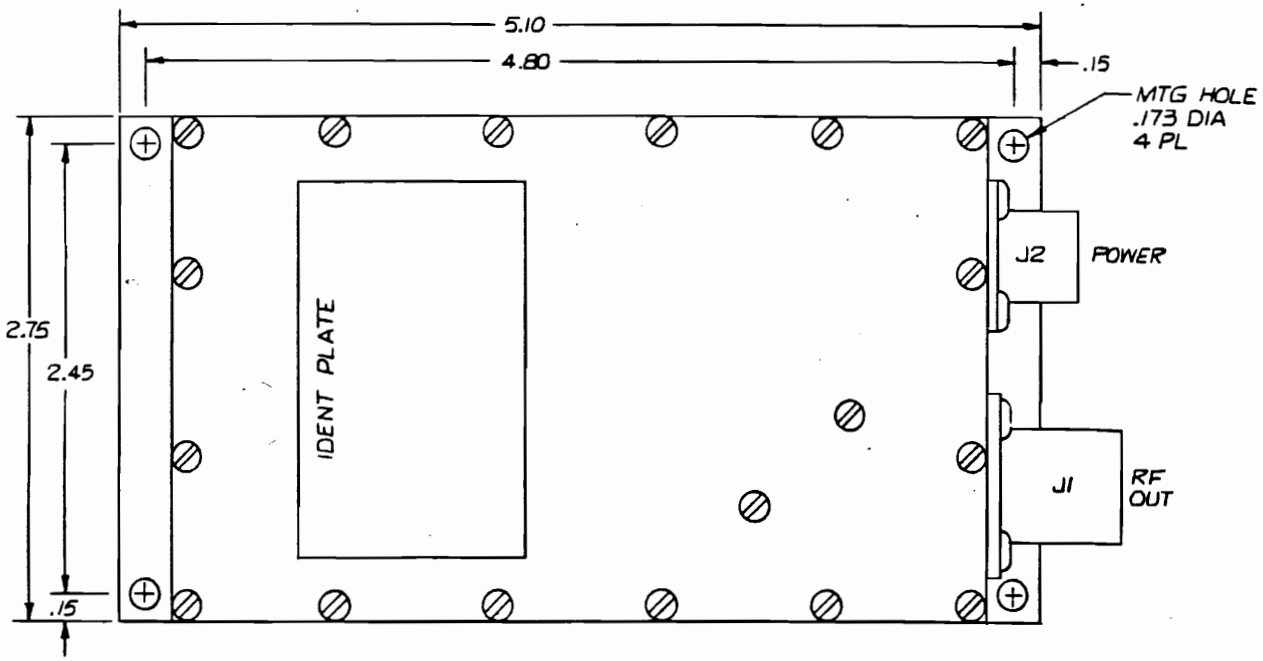

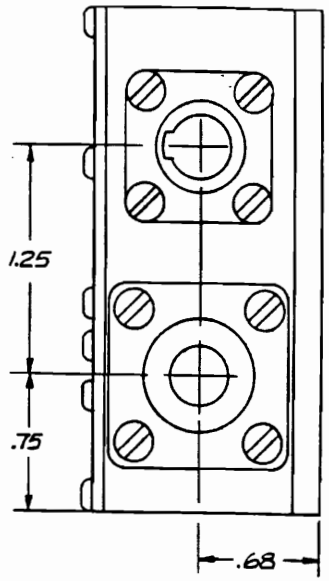

NOTES:
1. J1 DATA -
   TYPE: UG-58A/U
2. J2 DATA -
   TYPE: PT02E-8-4P
   MATING CONN: PT06E-8-4S
   PIN FUNCTIONS: A = 13.8 VDC
   B = MODULATION INPUT
   C = N/C
   D = CASE GND

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE.
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL: AL ALLOY

FINISH: IRRIDITE/ KRYLON

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN RCR	1/10/85
CHECKED	

MONITRON Corporation

OUTLINE -
TRANSMITTER, UHF, LOW PWR

SIZE	CODE IDENT NO	DRAWING NO
C		92C0003

SCALE 2/1 SHEET 1 OF 1

NEXT ASSY	USED ON

REVISIONS				
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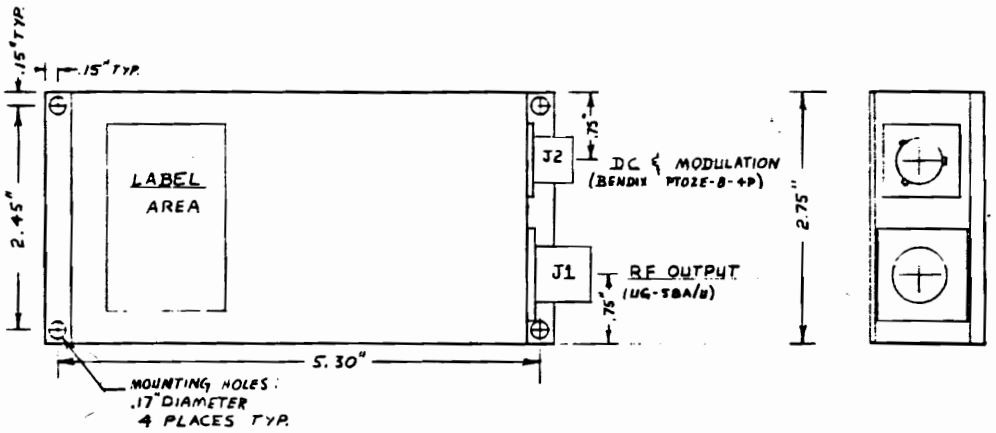
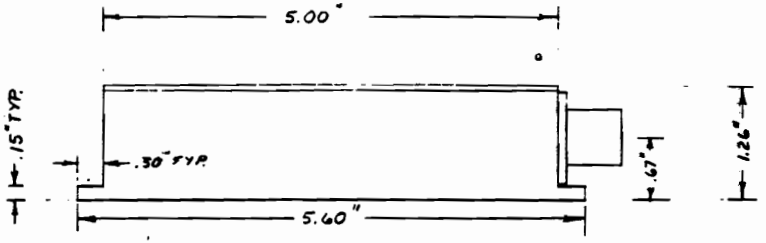




PIN CONNECTIONS:

A. +13.8 VDC
B MODULATION INPUT
C. N/C
D. MODULATION & POWER RETURN (GROUND)

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE.
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL: AL. ALLOY 2024-T3

FINISH: IRRIDITE / KRYLON

CONTRACT NO.

APPROVALS	DATE
DRAWN MDN	12-1-77
CHECKED	

MONITRON Corporation

OUTLINE, T45F-2
UHF TRANSMITTER

SIZE	CODE IDENT NO	DRAWING NO
C		92C0001

SCALE 1/1 SHEET 1 OF 1

	T45-F
NEXT ASSY	USED ON

DO NOT SCALE DRAWING

WARRANTY AND COMPANY POLICY:

Monitron Corporation warrants the above equipment against all material or manufacturing defects for a period of one year from the date of purchase. This warranty does not cover extraordinary instances resulting in damage to the equipment.

Monitron is constantly striving to improve its radio product line; For this reason, all published specifications, schematic diagrams, or other technical information relative to these products are subject to change without notice.

VIÐAUKI J

Bæklingur um loftnet

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

INVOICE

Remit to:
Monitron Corporation
Rt. 5, Box 459
Sand Springs, OK 74063
Tel. (918) 836-6831

INVOICE NO. **2750**

DATE 12/17/87

CUSTOMER ORDER NO. IR-27611

SOLD TO:
INNKAUPASTOFNUN RIKISINS
GOVERNMENT PURCHASING DEPT.
BORGARTUN 7, P.O. Box 1450
121 REYKJAVIK, ICELAND

SHIPPED TO:
INNKAUPASTOFNUN RIKISINS
GOVERNMENT PURCHASING DEPT.
BORGARTON 7, P.O. Box 1450
121 REYKJAVIK, ICELAND

OUR ORDER NO	SALESMAN	TERMS	FOB	DATE SHIPPED	SHIPPED VIA
87108		CAD through National Bank of Iceland (Landsbank)	Sand Springs, OK	see below	Burlington Air Frt.

ITEM NO	QUANTITY SHIPPED	DESCRIPTION	UNIT PRICE	AMOUNT USD
1	3 ea.	Antenna, Model CA7-460, Scala	185.00	555.00
		Total Transportation and Documentation		250.00
		Drop-shipped from factory.		
		SCALA ELECTRONIC CORPORATION MEDFORD, OREGON, USA MODEL CA7-460 FREQ. 450-470 MHZ SER# 1287-2 50 Ω		

Móttekið
22 DEC 1987
Innkaupastofnun ríkisins

A finance charge of 1½% per month will be charged on past due amounts.

SUB TOTAL	
TAX	
SHIPPING CHGS	
TOTAL	805.00

MONITRON Corporation
P.O. Box 27485 Tulsa, OK 74149-0485 (918) 836-6831

INVOICE

Remit to:
Monitron Corporation
Rt. 5, Box 459
Sand Springs, OK 74063
Tel. (918) 836-6831

INVOICE NO. 2751

DATE 12/17/87

CUSTOMER ORDER NO. IR-27611

SOLD TO: INNKAUPASTOFNUN RIKISINS
GOVERNMENT PURCHASING DEPT.
BORGARTUN 7, P.O. BOX 1450
121 REYKAJAVIK, ICELAND

SHIPPED TO: INNKAUPASTOFNUN RIKISINS
GOVERNMENT PURCHASING DEPT,
BORGARTON 7, P.O. BOX 1450
121 REYKJAVIK, ICELAND

OUR ORDER NO.	SALESMAN	TERMS	FOB	DATE SHIPPED	SHIPPED VIA
87108	Marvin Nelson	CAD through National Bank of Iceland (Landsbank)		12-21-87	Burlington Air Fr

ITEM NO.	QUANTITY SHIPPED	DESCRIPTION	UNIT PRICE	AMOUNT
1.	1 ea.	Transmitter, Model T45F-1, 150mw, 469.500MHz, S/N 1251	575.00	575.00
2.	1 ea.	Receiver, Model R45F, 469.500MHz, S/N 1251	575.00	575.00
	1 ea.	Mating Connector	N/C	
	1 ea.	Tuning Tool	N/C	
	1 set	Test Data, for each unit	N/C	
	1 ea	Instruction Manual, Transmitter	N/C	
	1 ea.	Instruction Manual, Receiver	N/C	

A finance charge of 1½% per month will be charged on past due amounts.

SUB TOTAL	1,150.00
TAX	
SHIPPING CHGS.	50.00
TOTAL	1,200.00

SCALA ELECTRONIC CORPORATION SO#1214-15 INVOICE

POST OFFICE BOX 4580 MEDFORD, OREGON 97501 (503) 779-6500

SOLD TO
MONITRON
P.O. BOX 27485
TULSA, OK 74149

SHIP TO
INNKAUPASTOFNUN RIKISINS
(GOVERNMENT PURCHASING DEPT)
BORGARTUNI 7, P.O. BOX 1450
121 REYKJAVIK, ICELAND

INVOICE NO.	INVOICE DATE	CUST. ORDER NUMBER	TERMS	SHIPPED VIA
		4359	2% 10/NET 30 DAYS	U.P.S. / AIR PPD&ADD

QUANTITY	DESCRIPTION	UNIT PRICE	EXTENSION	TOTAL
3	CA7-460 YAGI ANTENNA 450-470 MHZ 50 OHM N CONNECTOR			

PACKING LIST

REF: PO#IR-27611

WE HEREBY CERTIFY THAT THIS IS A CORRECT AND TRUE INVOICE, AND THAT THESE GOODS WERE MANUFACTURED IN THE U.S.A. FOR EXPORT TO ICELAND.

SCALA ELECTRONIC CORPORATION

1214

DC RETURN GOODS FOR CREDIT OR EXCHANGE WITHOUT OUR PERMISSION.

OVERDUE ACCOUNTS SUBJECT TO INTEREST CHARGE

CLAIMS OF ANY NATURE MUST BE MADE WITHIN 5 DAYS FROM RECEIPT OF GOODS.

VIÐAUKI K

Leyfisbréf frá Pósti og Síma

PÓST- OG SÍMAMÁLASTOFNUNIN

Tæknideild

Dagsetning vor: 24.02.1987
Dagsetning yðar:

Tilvísun vor: C-316/6260/87
Tilvísun yðar:

Orkustofnun,
-hr Einar Hrafnkell Haraldsson
Grensásvegi 9
108 REYKJAVÍK.

Með tilvísun í bréf yðar dags 11.02.1987 heimilar Póst- og símamálastofnunin yður notkun tíðnanna 469.500 og 469.650 MHz. Tíðnin 469.500 MHz fyrir sendingu úr nágrenni Reykjavíkur að Grensásveg 9 og 469.650 MHz er fyrir notkun á Kröflusvæðinu. Að auki er heimild fyrir notkun 469.500 MHz á Kröflusvæðinu í tilfellum ef hitt sambandið bilar.

Leyfilegt sendiafl er 150 mW.

Athuga ber að sendar þurfa að koma í tegundarprófun hjá Radíóeftirlitinu Sölvhólsgötu 11, Reykjavík.

Vinsamlegast látið okkur vita er þér vitið um nákvæma staðsetningu senda.

Virðingarfyllst,

Kristján Bjartmarsson,
deildarverkfræðingur

Hörður R. Harðarson,
verkfræðingur

8

Póstfang	Aðsetur	Sími (TP)	Símnefni (TG)	Telex (TX	Myndsendir
150 REYKJAVÍK	við Austurvöll	(91) 2 60 00	Postgen Gentel	2000 gentel.is	(91) 2 82 45

PÓST- OG SÍMAMÁLASTOFNUNIN

Tæknideild

Dagsetning vor: 11.03.1988
Dagsetning yðar:

Tilvísun vor: C-319/6565/88
Tilvísun yðar:

Orkustofnun
Grensásvegi 9

108 REYKJAVIK.

Póst- og símamálastofnunin hefur að ósk yðar prófað sendi af gerðinni Monitron T45F-1 framleiddum af Monitron Corporation í Bandaríkjunum.

Sendirinn uppfyllir ekki að öllu leyti kröfur um óæskilegar útgeislanir en stofnunin fellst á að veita heimild fyrir notkun á þessum sendi með staðsetningu á Leirhnjúk í Mývatnssveit.

Stofnunin mun senda yður reikning fyrir umfjöllunina innan tíðar.

Virðingarfyllst,

Gústav Arnar,
yfirverkfræðingur

8

Póstfang: 150 REYKJAVÍK
Aðsetur: við Austurvöll
Sími (TP): (91) 2 60 00
Símnefni (TG): Postgen Gentel
Telex (TX): 2000 gentel is
Myndsendir: (91) 2 82 45

VIÐAUKI L

Upplýsingar um afbrigðilegar rásir

YSI PRECISION THERMISTOR

LN 7279

YSI 44030

RESISTANCE 3000 OHMS @25°C

Interchangeability: ±0.1°C (See Tolerance Curves).

Max. Operating Temp: 100°C (212°F). Extended operation or continued cycling above 75° will cause thermistor to eventually exceed tolerances.

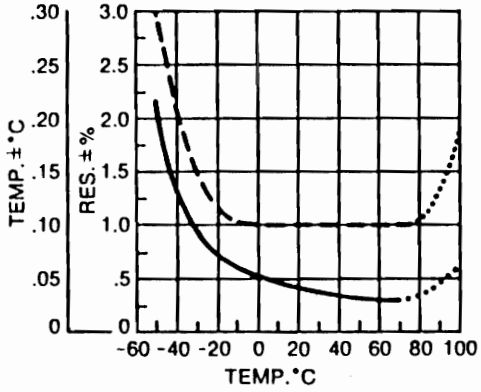
Time Constant, Max: 1 sec. in well stirred oil, 10 sec. in still air. Time constant is the time required for a thermistor to indicate 63% of a newly impressed temperature.

Dissipation Constant, Min: 8mW/°C in well stirred oil, 1mW/°C in still air. Dissipation constant is the power in milliwatts to raise a thermistor 1°C above surrounding temperature.

Color Code: Orange epoxy body, black end.

Storage Temperature: -80° to +75°C (-112° to +167°F).

Tolerance Curves: The following curves indicate conformance to standard resistance temperature values as a % of resistance, and as a maximum interchangeability error expressed as temperature.



WARNING

Use heat sinks (needle nose plyers, etc.) when soldering or welding to thermistor leads.

Industrial Division
Yellow Springs Instrument Co.
Yellow Springs, Ohio 45387, U.S.A.
Phone 513-767-7241

ITEM 003300 P/N B44530-C Printed in U.S.A. AB

YSI PRECISION THERMISTOR

RESISTANCE VERSUS TEMPERATURE —40° to +100°C

TEMP°C	RES	TEMP°C	RES	TEMP°C	RES	TEMP°C	RES
— 40	100.9K	— 10	16.59K	+ 20	3748	+ 50	1080
39	94.46K	9	15.72K	21	3583	51	1040
38	88.44K	8	14.89K	22	3426	52	1002
37	82.85K	7	14.12K	23	3277	53	964.6
36	77.64K	6	13.38K	24	3135	54	929.3
35	72.79K	5	12.70K	25	3000	55	895.4
34	68.28K	4	12.05K	26	2872	56	863.0
33	64.07K	3	11.43K	27	2750	57	831.9
32	60.15K	2	10.85K	28	2633	58	802.1
31	56.49K	1	10.31K	29	2523	59	773.5
— 30	53.08K	— 0	9795	+ 30	2417	+ 60	746.0
29	49.89K	+ 1	9309	31	2317	61	719.7
28	46.92K	2	8850	32	2221	62	694.4
27	44.14K	3	8416	33	2130	63	670.2
26	41.54K	4	8006	34	2042	64	646.9
25	39.11K	5	7618	35	1959	65	624.6
24	36.84K	6	7252	36	1880	66	603.1
23	34.71K	7	6905	37	1805	67	582.4
22	32.72K	8	6576	38	1733	68	562.7
21	30.86K	9	6265	39	1664	69	543.6
— 20	29.11K	+ 10	5971	+ 40	1598	+ 70	525.3
19	27.47K	11	5692	41	1535	71	507.7
18	25.94K	12	5428	42	1475	72	490.8
17	24.50K	13	5177	43	1418	73	474.5
16	23.15K	14	4939	44	1363	74	458.9
15	21.88K	15	4714	45	1310	75	443.8
14	20.69K	16	4500	46	1260	76	429.3
13	19.57K	17	4297	47	1212	77	415.4
12	18.51K	18	4105	48	1167	78	402.0
11	17.52K	19	3922	49	1123	79	389.1
						+ 80	376.6
						81	364.7
						82	353.1
						83	342.0
						84	331.3
						85	321.0
						86	311.0
						87	301.4
						88	292.2
						89	283.3
						+ 90	274.7
						91	266.4
						92	258.4
						93	250.6
						94	243.2
						95	236.0
						96	229.0
						97	222.3
						98	215.8
						99	209.5
						+ 100	203.5

LINEAR TECHNOLOGY

LT1080/LT1081

5V Powered RS232 Driver/ Receiver with Shutdown

FEATURES

- Operates on Single 5V Power Supply
- Generates ±9V Supplies with Only 1μF Capacitors
- Fully Protected Against Output Overloads
- RS232 Outputs can be Forced ±30V without Damage
- Three-state Outputs are High Impedance when Off
- Bipolar Circuitry; No Latch Up
- ±30V Receiver Input Range
- Can Power Additional RS232 Drivers such as LT1039
- No Supply Current in Shutdown
- Meets All RS232 Specifications
- 16 Pin Version without Shutdown Available
- Available in SO Package

APPLICATIONS

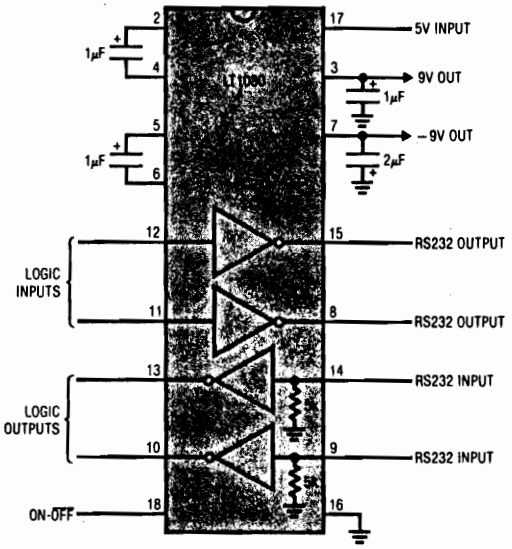
- Portable Computers
- Battery Powered RS232 Systems
- Power Supply Generator
- Terminals
- Modems

DESCRIPTION

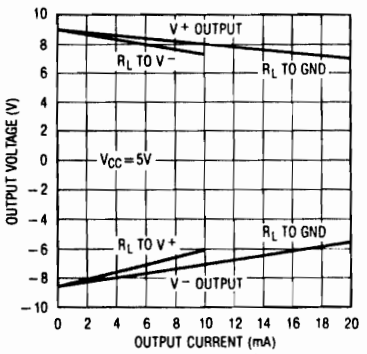
The LT1080 is a dual RS232 driver/receiver which includes a capacitive voltage generator to supply RS232 voltage levels from a single 5V supply. Each receiver will accept up to ±30V input and can drive either TTL or CMOS logic. The RS232 drivers accept logic inputs and output RS232 voltage levels. The driver outputs are fully protected against overload and can be shorted to ground or up to ±30V without damage. Additionally, when the system is in the SHUTDOWN mode the driver and receiver outputs are at a high impedance allowing data line sharing. Bipolar circuitry makes this driver/receiver exceptionally rugged against overloads or ESD damage.

The power supply generator doubles the 5V input supply to obtain 9V, and then inverts the 9V to obtain −8.5V. Up to 15mA of external current is available to power additonal RS232 drivers or other external circuitry. The SHUTDOWN mode disables the supply generators and reduces input supply current to zero. A version of the LT1080, the LT1081, is available without shutdown for 16 pin applications.

TYPICAL APPLICATION



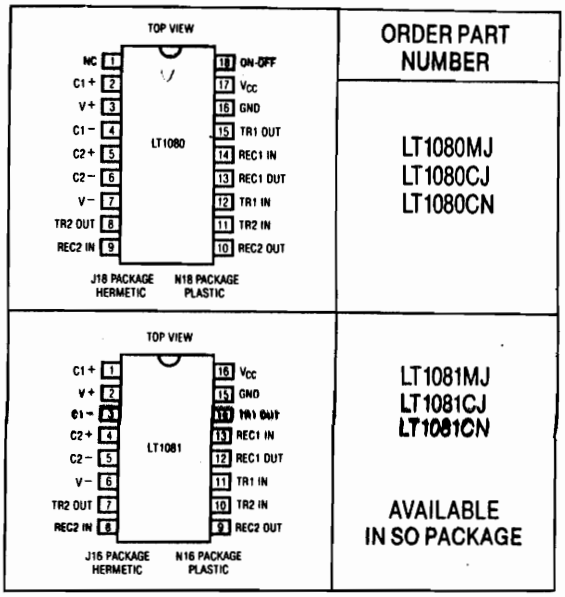
Supply Generator Outputs



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 6V
V^+ 12V
V^- ..... −12V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −30V to 30V
  On-$\overline{Off}$ Pin ..... GND to 12V
Output Voltage
  Driver ..... V^- + 30V to V^+ − 30V
  Receiver ..... −0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 Seconds
  V^- ..... 30 Seconds
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1080M ..... −55°C to 125°C
  LT1080C ..... 0°C to 70°C
  Guaranteed Functional ..... −25°C to 85°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1080MJ LT1080CJ LT1080CN
LT1081MJ LT1081CJ LT1081CN AVAILABLE IN SO PACKAGE

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Driver							
Output Voltage Swing	Load = 3k to GND Both Outputs.	Positive Negative	● ●	5.0 −5.0	7.3 −6.5		V V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High) Input High Level (V_{OUT} = Low)		● ●	 2.0	1.4 1.4	0.8	V V
Logic Input Current	$V_{IN} \geq 2.0V$ $V_{IN} \leq 0.8V$		● ●	 	5 5	20 20	µA µA
Output Short Circuit Current	Sourcing Current, V_{OUT} = 0V Sinking Current, V_{OUT} = 0V		 	7 −7	12 −12		mA mA
Output Leakage Current	SHUTDOWN (Note 2), V_{OUT} = ±30V		●		10	100	µA
Slew Rate	R_L = 3kΩ, C_L = 51pF			4	15	30	V/µs
Receiver							
Input Voltage Thresholds	Input Low Threshold, (V_{OUT} = High) Input High Threshold, (V_{OUT} = Low)		● ●	0.2 	1.3 1.7	 3.0	V V
Hysteresis			●	0.1	0.4	1.0	V
Input Resistance				3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160µA (V_{CC} = 5V)		● ●	 3.5	0.2 4.8	0.4 	V V
Output Short Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		 	−10 0.6	−20 1	 	mA mA
Output Leakage Current	SHUTDOWN (Note 2), 0V ≤ V_{OUT} ≤ V_{CC}		●		1	10	µA

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Generator (Note 3)							
V+ Output Voltage	I_{OUT} = 0mA I_{OUT} = 10mA I_{OUT} = 15mA			8 7 6.5	9 8 7.5		V V V
V− Output Voltage	I_{OUT} = 0mA I_{OUT} = −10mA I_{OUT} = −15mA			−7.5 −5.5 −5	−8.5 −6.5 −6		V V V
Supply Current			●		10	22	mA
Supply Leakage Current (V_{CC})	SHUTDOWN (Note 2)	(LT1080 Only)	●		1	100	µA
On-$\overline{\text{Off}}$ Pin Current	0V ≤ $V_{ON\text{-}\overline{OFF}}$ ≤ 5V	(LT1080 Only)	●	−15		80	µA
Supply Rise Time	(Note 4)	(LT1080 Only)			1		ms

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade or −55°C ≤ T_A ≤ 125°C for military grade devices). The LT1080/LT1081 is guaranteed functional by design for −25°C ≤ T_A ≤ 85°C.

Note 1: These parameters apply for 4.5V ≤ V_{CC} ≤ 5.5V and $V_{ON\text{-}\overline{OFF}}$ = 3V, unless otherwise specified.

Note 2: $V_{ON\text{-}\overline{OFF}}$ = 0.4V for −55°C ≤ T_A ≤ 100°C, and $V_{ON\text{-}\overline{OFF}}$ = 0.2V for 100°C ≤ T_A ≤ 125°C. (LT1080 only)

Note 3: Unless otherwise specified, V_{CC} = 5V, external loading of V+ and V− equals zero and the driver outputs are low (inputs high).

Note 4: Time from either SHUTDOWN high or power on until V+ ≥ 6V and V− ≤ −6V. All external capacitors are 1µF.

PIN FUNCTIONS

V_{CC} (Pin 17): Input supply pin. Supply current drops to zero in the SHUTDOWN mode.

GND (Pin 16): Ground pin.

On-$\overline{\text{Off}}$ (Pin 18): Controls the operation mode of the LT1080 and is TTL/CMOS compatible. A logic low puts the device in the SHUTDOWN mode which reduces input supply current to zero and places both driver and receiver outputs in a high impedance state. A logic high fully enables the device.

V+ (Pin 3): Positive supply for RS232 drivers. V+ ≈ 2V_{CC} − 1.5V. Requires an external capacitor (≥ 1µF) for charge storage. May be loaded (up to 15mA) for external system use. Loading does reduce V+ voltage (see graphs.) Capacitor may be tied to ground or +5V input supply.

V− (Pin 7): Negative supply for RS232 drivers. V− ≈ −(2V_{CC} − 2.5V). Requires an external capacitor (≥ 1µF) for charge storage. May be loaded (up to −15mA) for external system use. Loading does reduce V− voltage (see graphs).

TR1 IN; TR2 IN (Pins 12, 11): RS232 driver input pins. Inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

TR1 OUT; TR2 OUT (Pins 15, 8): Driver outputs with RS232 voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode or when power is off (V_{CC} = 0V) to allow data line sharing. Outputs are fully short circuit protected from V− + 30V to V+ − 30V with power on, off, or in the SHUTDOWN mode. Typical output breakdowns are greater than ±45V and higher applied voltages will not damage the device if moderately current limited.

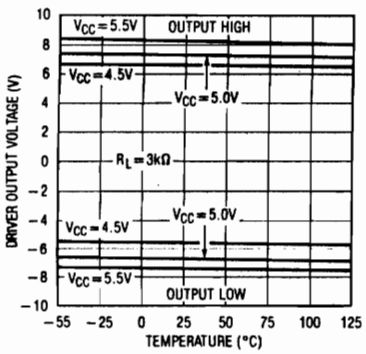
REC1 IN; REC2 IN (Pins 14, 9): Receiver inputs. Accepts RS232 voltage levels (±30V) and has 0.4V of hysteresis to provide noise immunity. Input impedance is nominally 5kΩ.

REC1 OUT; REC2 OUT (Pins 13, 10): Receiver outputs with TTL/CMOS voltage levels. Outputs are in a high impedance state when in the SHUTDOWN mode to allow data line sharing. Outputs are fully short circuit protected to ground or V_{CC} with power on, off, or in the SHUTDOWN mode.

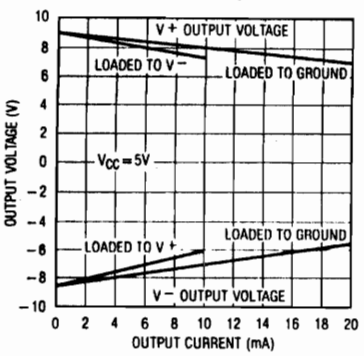
C1+; C1−; C2+; C2− (Pins 2, 4, 5, 6): No user applications. Requires an external capacitor (≥ 1µF) from C1+ to C1− and another from C2+ to C2−.

TYPICAL PERFORMANCE CHARACTERISTICS

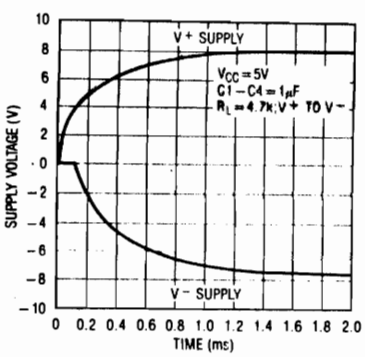
Driver Output Voltage



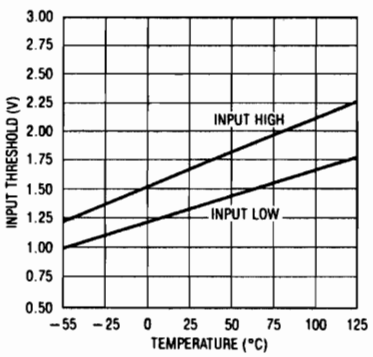
Supply Generator Outputs



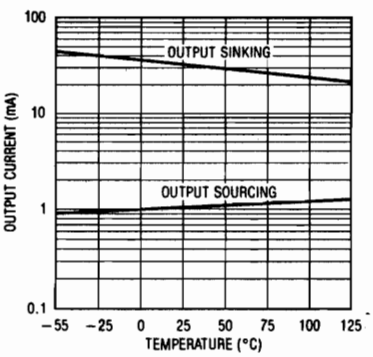
Supply Generation from V_{CC} or Shutdown



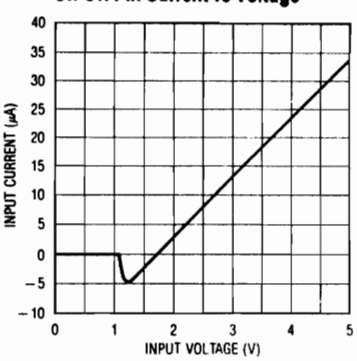
Receiver Input Thresholds



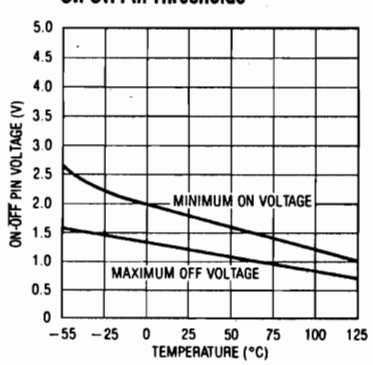
Receiver Output Short Circuit Current



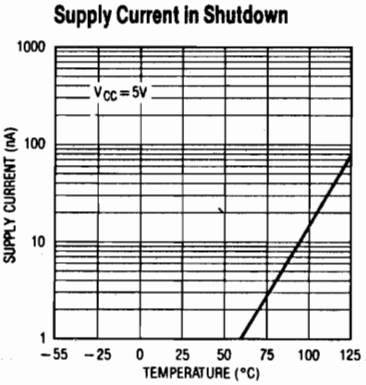
On-$\overline{\text{Off}}$ Pin Current vs Voltage



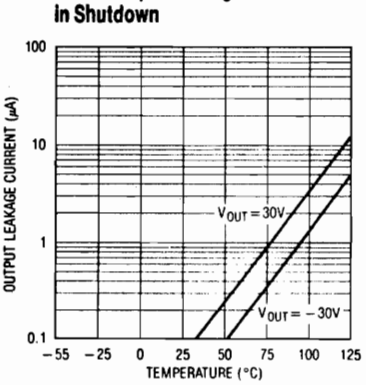
On-$\overline{\text{Off}}$ Pin Thresholds



Supply Current in Shutdown

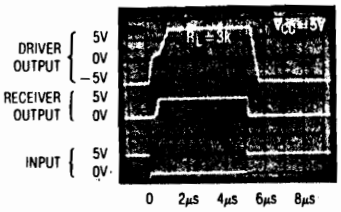


Driver Output Leakage in Shutdown

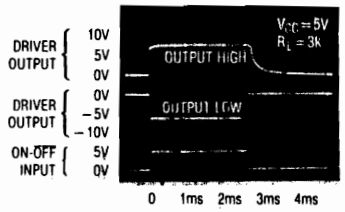


TYPICAL PERFORMANCE CHARACTERISTICS

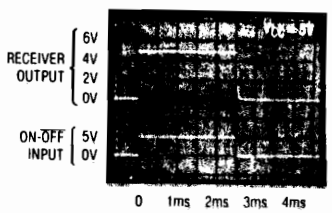
Output Waveforms



Shutdown to Driver Output

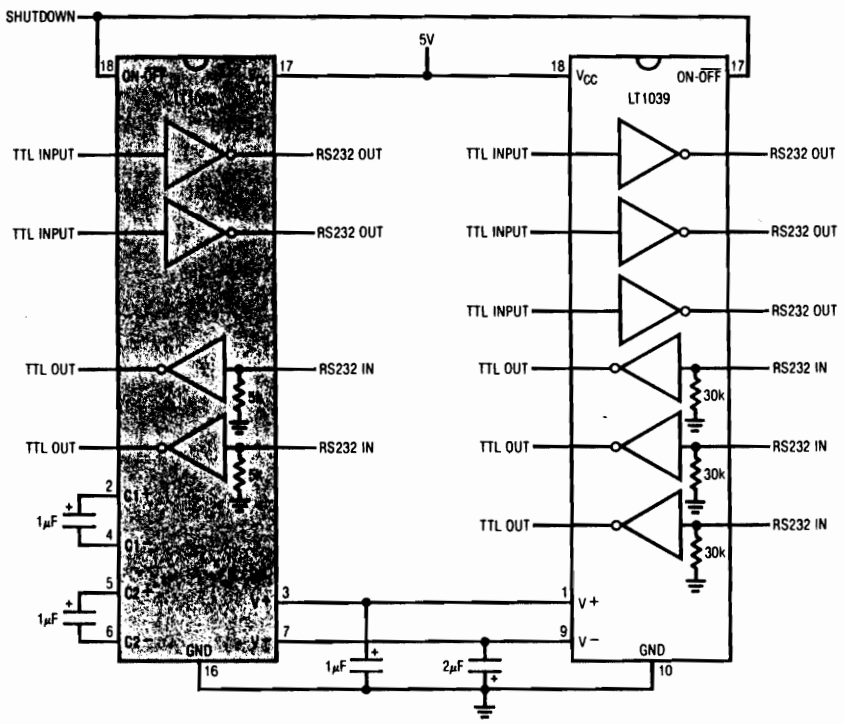


Shutdown to Receiver Output



TYPICAL APPLICATION

Supporting an LT1039 (Triple Driver/Receiver)



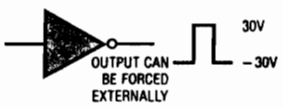
APPLICATION HINTS

The driver output stage of the LT1080 offers significantly improved protection over older bipolar and CMOS designs. In addition to current limiting, the driver output can be externally forced to ±30V with no damage or excessive current flow, and will not disrupt the supplies. Some drivers have diodes connected between the outputs and the supplies, so externally applied voltages can cause excessive supply voltage to develop.

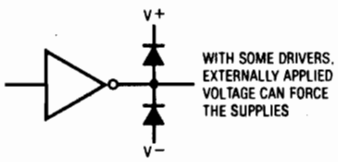
Placing the LT1080 in the SHUTDOWN mode (Pin 18 low) puts both the driver and receiver outputs in a high impedance state. This allows data line sharing and transceiver applications.

The SHUTDOWN mode also drops input supply current (V_{CC}; Pin 17) to zero for power-conscious systems.

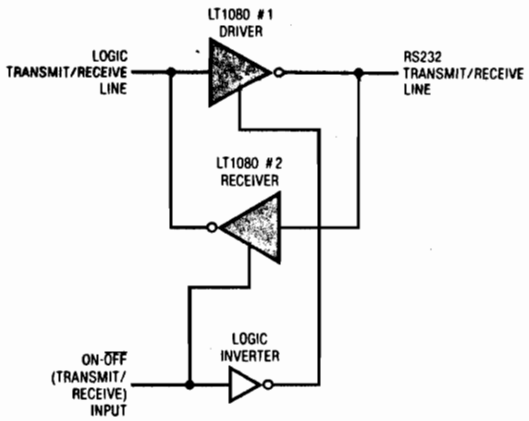
LT1080/LT1081 Driver



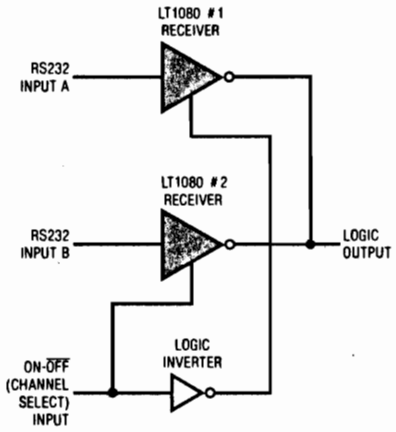
Older RS232 Drivers and CMOS Drivers



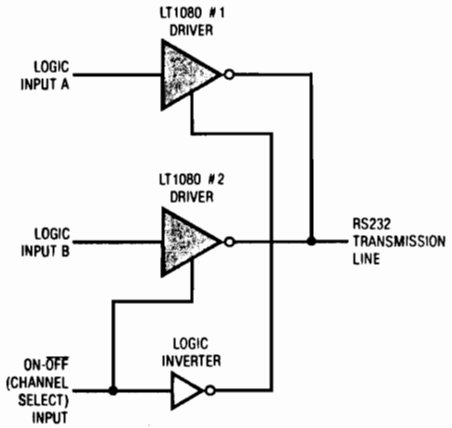
Transceiver



Sharing a Receiver Line

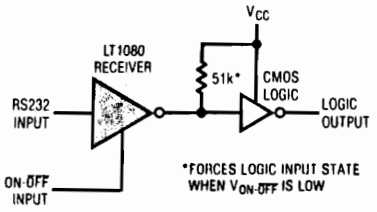


Sharing a Transmitter Line

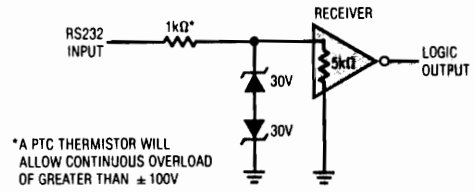


APPLICATION HINTS

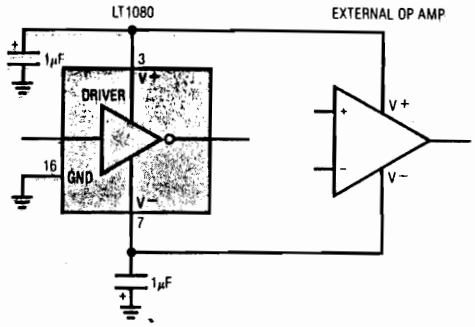
When driving CMOS logic from a receiver that will be used in the SHUTDOWN mode and there is no other active receiver on the line, a 51k resistor can be placed from the logic input to V_{CC} to force a definite logic level when the receiver output is in a high impedance state.



To protect against receiver input overloads in excess of ±30V, a voltage clamp can be placed on the data line and still maintain RS232 compatibility.

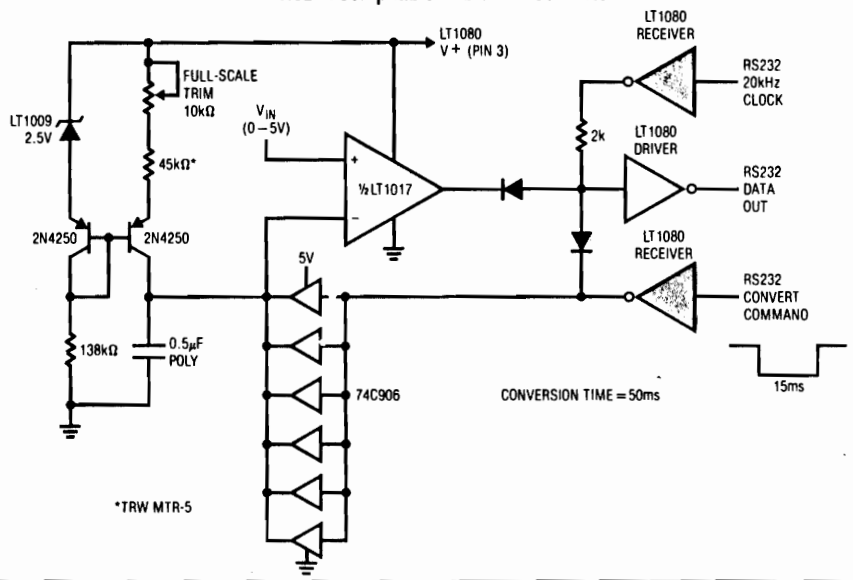


The generated driver supplies (V+ and V−) may be used to power external circuitry such as other RS232 drivers or op amps. They should be loaded with care, since excessive loading can cause the generated supply voltages to drop causing the RS232 driver output voltages to fall below RS232 requirements. See the graph "Supply Generator Outputs" for a comparison of generated supply voltage versus supply current.



TYPICAL APPLICATION

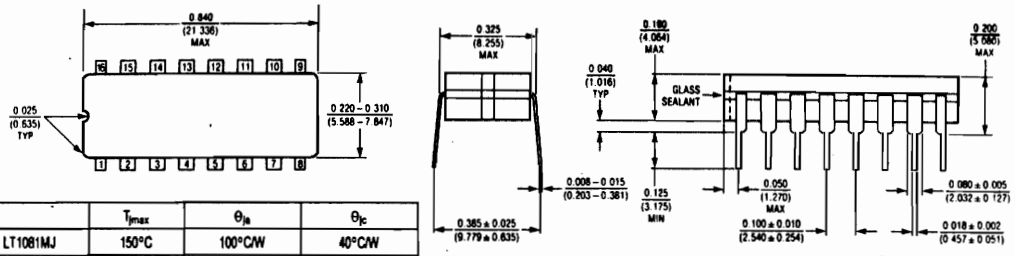
RS232 Compatible 10-Bit A-D Converter



PACKAGE DESCRIPTION

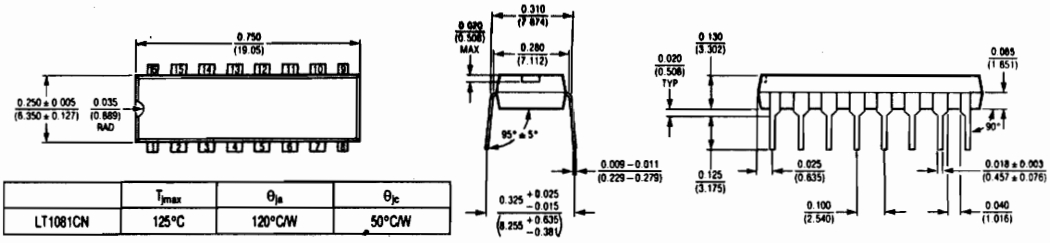
Dimensions in inches (millimeters) unless otherwise noted.

J16 Package Ceramic DIP



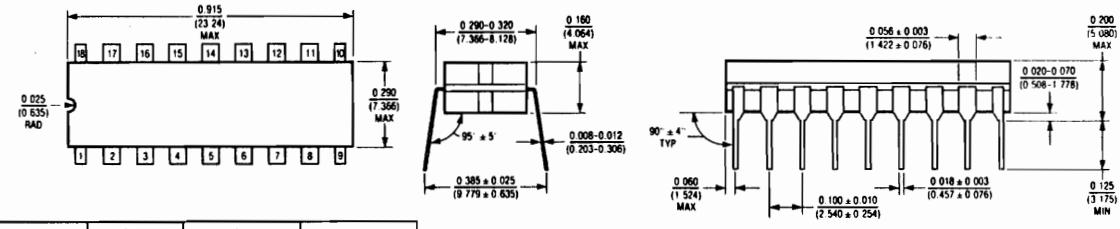
	T_{jmax}	θ_{ja}	θ_{jc}
LT1081MJ	150°C	100°C/W	40°C/W
LT1081CJ	150°C	100°C/W	40°C/W

N16 Package Plastic DIP



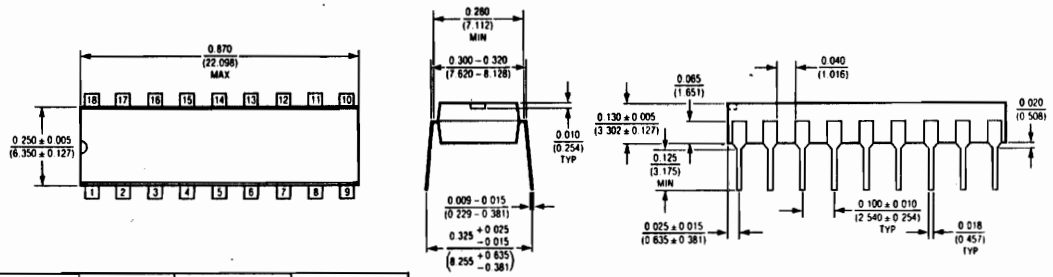
	T_{jmax}	θ_{ja}	θ_{jc}
LT1081CN	125°C	120°C/W	50°C/W

J18 Package Ceramic DIP



	T_{jmax}	θ_{ja}	θ_{jc}
LT1080MJ	150°C	100°C/W	40°C/W
LT1080CJ	150°C	100°C/W	40°C/W

N18 Package Plastic DIP



	T_{jmax}	θ_{ja}	θ_{jc}
LT1080CN	125°C	120°C/W	50°C/W

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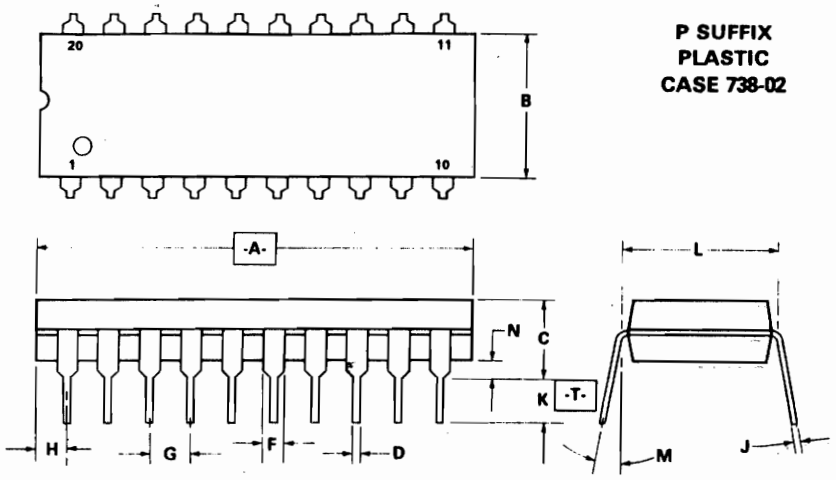
1630 McCarthy Blvd., Milpitas, CA 95035-7487 • (408) 432-1900
FAX: (408) 434-0507 • TELEX: 499-3977

IM/GP 587 2K REV A

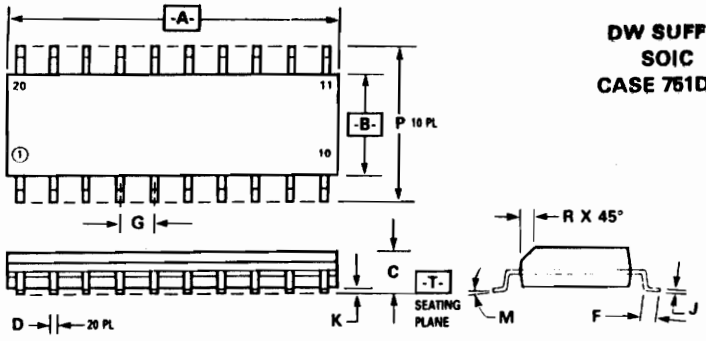
PACKAGE DIMENSIONS



P SUFFIX
PLASTIC
CASE 738-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.65	27.18	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.94	4.57	0.155	0.180
D	0.38	0.56	0.015	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.65 NOM		0.065 NOM	
J	0.20	0.38	0.008	0.015
K	2.79	3.56	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

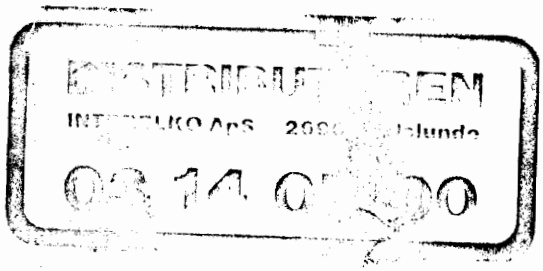
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ ⌀ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM "B" DOES NOT INCLUDE MOLD FLASH.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



DW SUFFIX
SOIC
CASE 751D-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.509
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. POSITIONAL TOLERANCE FOR D DIMENSION (20 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ
3. POSITIONAL TOLERANCE FOR P DIMENSION (10 PLACES):
   ⌖ | 0.25 (0.010) Ⓜ | B Ⓜ
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: MILLIMETER
6. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
7. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.



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AVENUE GÉNÉRAL EISENHOWER, 31023 TOULOUSE CEDEX, FRANCE

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

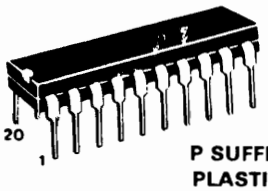
MC145442
MC145443

Advance Information

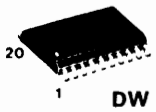
Single Chip 300 Baud Modem

The MC145442 and MC145443 silicon-gate CMOS single-chip low-speed modems contain a complete frequency shift keying (FSK) modulator, demodulator, and filter. These devices are compatible with CCITT V.21 (MC145442) and Bell 103 (MC145443) specifications. Both devices provide full-duplex or half-duplex 300 baud data communicaton over a pair of telephone lines. They also include a carrier detect circuit for the demodulator section and a duplexer circuit for direct operation on a telephone line through a simple transformer.

- MC145442 Compatible with CCITT V.21
- MC145443 Compatible with Bell 103
- Low-Band and High-Band Bandpass Filters On-Chip
- Simplex, Half-Duplex, and Full-Duplex Operation
- Originate and Answer Mode
- Analog Loopback Configuration for Self Test
- Hybrid Network Function On-Chip
- Carrier Detect Circuit On-Chip
- Adjustable Transmit Level and $\overline{CD}$ Delay Timing
- On-Chip Crystal Oscillator (3.579 MHz)
- Single +5 Volt Power Supply Operation
- Internal Mid-Supply Generator
- Power-Down Mode
- Pin Compatible with MM74HC943
- Capable of Driving −9 dBm into a 600-Ohm Load

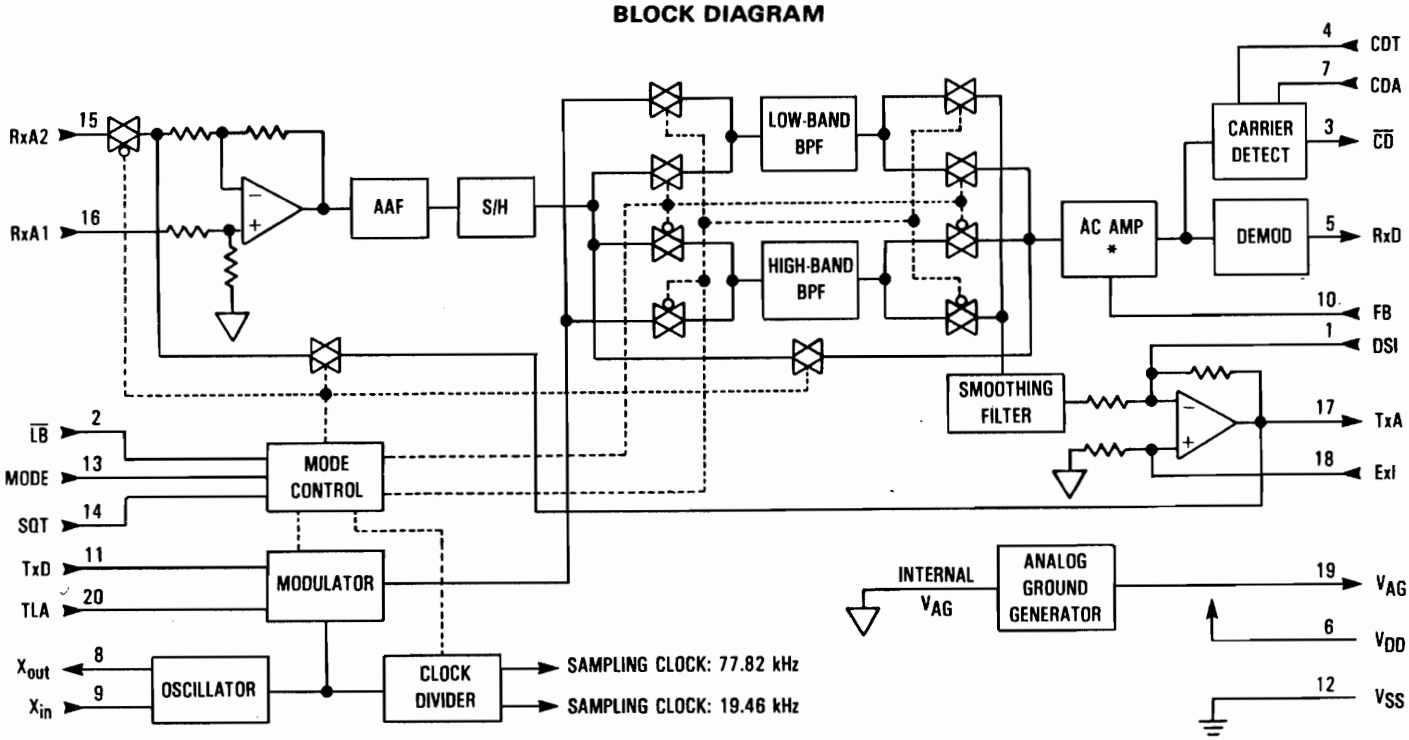


P SUFFIX
PLASTIC
CASE 738



DW SUFFIX
SOIC
CASE 751D

BLOCK DIAGRAM



*Refer to the FB pin description.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.5 to 7.0	V
DC Input Voltage	V_{in}	−0.5 to V_{DD}+0.5	V
DC Output Voltage	V_{out}	−0.5 to V_{DD}+0.5	V
Clamp Diode Current, per Pin	I_{IK}, I_{OK}	±20	mA
DC Output Current, per Pin	I_{out}	±28	mA
Power Dissipation	PD	500	mW
Operating Temperature Range	T_A	−40 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

This device contains circuitry to protect against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused outputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	4.5	5.5	V
DC Input or Output Voltage	V_{in}, V_{out}	0	V_{DD}	V
Input Rise or Fall Time	t_r, t_f	—	500	ns
Crystal Frequency*	$f_{crystal}$	3.2	5.0	MHz

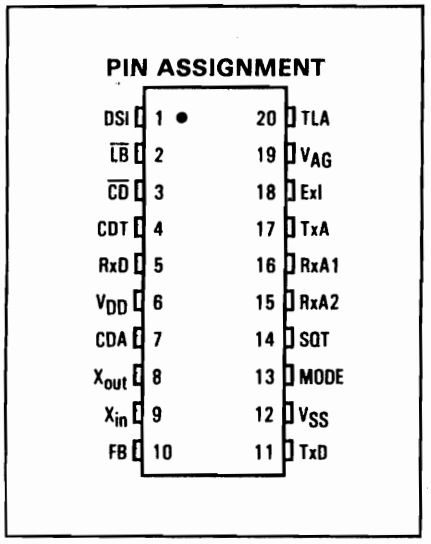
*Changing the crystal frequency from 3.579 MHz will change the output frequencies. The change in output frequency will be proportional to the change in crystal frequency.

DC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = −40 to 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	$\overline{LB}$	V_{IH}	V_{DD} − 0.8	—	—	V
	X_{in}, TxD, Mode, SQT		3.15	—	—	
Low-Level Input Voltage	$\overline{LB}$	V_{IL}	—	—	0.8	V
	X_{in}, TxD, Mode, SQT		—	—	1.1	
High-Level Output Voltage		V_{OH}				V
I_{OH} = 20 μA	$\overline{CD}$, RxD		V_{DD} − 0.1	—	—	
I_{OH} = 2 mA	$\overline{CD}$, RxD		3.7	—	—	
I_{OH} = 20 μA	X_{out}		—	V_{DD} − 0.05	—	
Low-Level Output Voltage		V_{OL}				V
I_{OL} = 20 μA	$\overline{CD}$, RxD		—	—	0.1	
I_{OL} = 2 mA	$\overline{CD}$, RxD		—	—	0.4	
I_{OL} = 20 μA	X_{out}		—	0.05	—	
Input Current	$\overline{LB}$, TxD, Mode, SQT	I_{in}	—	—	±1.0	μA
	RxA1, RxA2		—	10	±12	
	X_{in}		—	—	±10	
Quiesent Supply Current X_{in} or $f_{crystal}$ = 3.579 MHz		I_{DD}	—	7	10	mA
Power-Down Supply Current			—	200	300	μA
Input Capacitance	X_{in}	C_{in}	—	10	—	pF
	All Other Inputs		—	—	10	
V_{AG} Output Voltage (I_O = ±10 μA)		V_{AG}	2.4	2.5	2.6	V
CDA Output Voltage (I_O = ±10 μA)		V_{CDA}	1.1	1.2	1.3	V
Line Driver Feedback Resistor		R_f	10	20	30	kΩ

AC ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = −40 to 85°C, Crystal Frequency = 3.579 MHz ± 0.1%; See Figure 1)

Characteristic		Min	Typ	Max	Unit
TRANSMITTER					
Power Output on TxA RL = 1.2 kΩ, R_{TLA} = ∞ RL = 1.2 kΩ, R_{TLA} = 5.5 kΩ		 −13 −10	 −12 −9	 −11 −8	dBm
Second Harmonic Power RL = 1.2 kΩ		—	−56	—	dBm
RECEIVE FILTER AND HYBRID					
Hybrid Input Impedance RxA1, RxA2		40	50	—	kΩ
FB Output Impedance		—	16	—	kΩ
Adjacent Channel Rejection		−48	—	—	dBm
DEMODULATOR					
Receive Carrier Amplitude		−48	—	−12	dBm
Dynamic Range		—	36	—	dB
Bit Jitter (S/N = 30 dB, Input = −38 dBm, Bit Rate = 300 baud)		—	100	—	μs
Bit Bias		—	5	—	%
Carrier Detect Threshold (CDA = 1.2 V or CDA grounded through a 0.1 μF capacitor)	On to Off Off to On	— —	−44 −47	— —	dBm



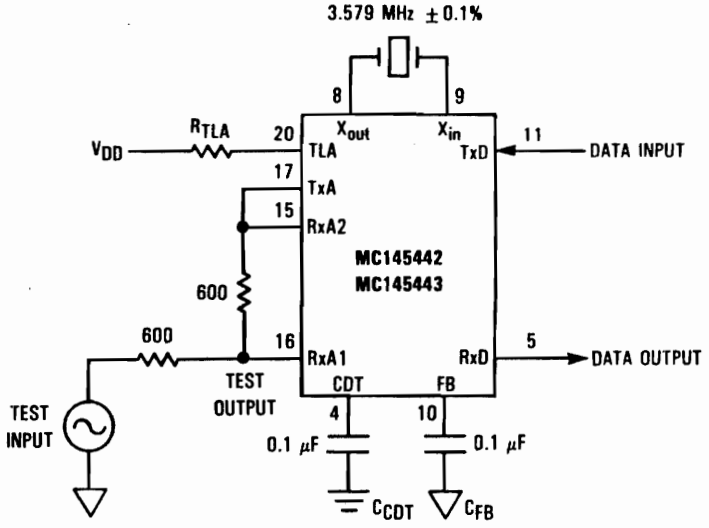


Figure 1. AC Characteristics Evaluation Circuit

PIN DESCRIPTIONS

V_{DD} — POSITIVE POWER SUPPLY (PIN 6)

This pin is normally tied to 5.0 V.

V_{SS} — NEGATIVE POWER SUPPLY (PIN 12)

This pin is normally tied to 0 V.

V_{AG} — ANALOG GROUND (PIN 19)

Analog ground is internally biased to $(V_{DD} - V_{SS})/2$. This pin must be decoupled by a capacitor from V_{AG} to V_{SS} and a capacitor from V_{AG} to V_{DD}. Analog ground is the common bias line used in the switched capacitor filters, limiter, and slicer in the demodulation circuitry.

TLA — TRANSMIT LEVEL ADJUST (PIN 20)

This pin is used to adjust the transmit level. Transmit level adjustment range is typically from −12 dBm to −9 dBm. (See Applications Information.)

TxD — TRANSMIT DATA (PIN 11)

Binary information is input to the transmit data pin. Data entered for transmission is modulated using FSK techniques. A logic high input level represents a mark and a logic low represents a space. (See Table 1.)

Table 1. Bell 103 and CCITT V.21 Frequency Characteristics

Bell 103 (MC145443)				
Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz
CCITT V.21 (MC145442)				
Data	Originate Mode		Answer Mode	
	Transmit	Receive	Transmit	Receive
Space	1180 Hz	1850 Hz	1850 Hz	1180 Hz
Mark	980 Hz	1650 Hz	1650 Hz	980 Hz

NOTE: Actual frequencies may be ±5 Hz assuming a 3.579545 MHz crystal is used.

TxA—TRANSMIT CARRIER (PIN 17)

This is the output of the line driver amplifier. The transmit carrier is the digitally synthesized sine wave output of the modulator derived from a crystal oscillator reference. When a 3.579 MHz crystal is used the frequency outputs shown in Table 1 apply. (See Applications Information.)

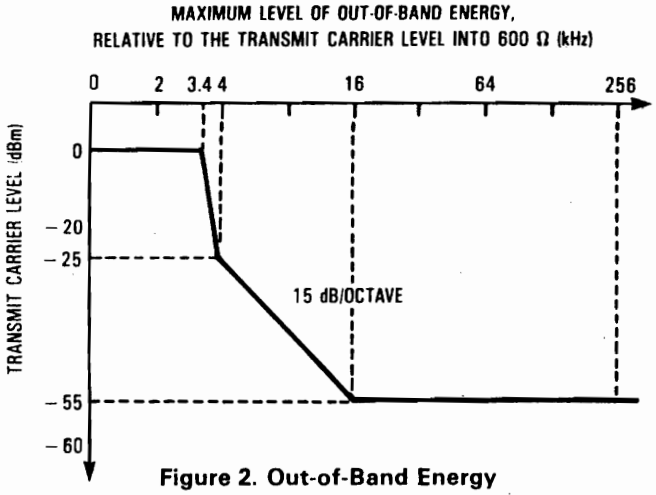


Figure 2. Out-of-Band Energy

ExI—EXTERNAL INPUT (PIN 18)

The external input is the noninverting input to the line driver. It is provided to combine an auxiliary audio signal or speech signal to the phone line using the line driver. This pin should be connected to V_{AG} if not used. The average level must be the same as V_{AG} to maintain proper operation. (See Applications Information.)

DSI—DRIVER SUMMING INPUT (PIN 1)

The driver summing input may be used to connect an external signal, such as a DTMF dialer, to the phone line. A series resistor, R_{DSI}, is needed to define the voltage gain A_V (see Applications Information and Figure 6). When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (pin 14) to a logic high level. The voltage gain, A_V, is calculated by the formula $A_V = -R_f/R_{DSI}$ (where $R_f \approx 20\ k\Omega$). For example, a 20 kΩ resistor for R_{DSI} will provide unity gain ($A_V = -20\ k\Omega/20\ k\Omega = -1$). This pin MUST be left OPEN if not used.

RxD—RECEIVE DATA (PIN 5)

The receive data output pin presents the digital binary data resulting from the demodulation of the receive carrier. If no carrier is present, $\overline{CD}$ high, the receive data output (RxD) is clamped high.

RxA2, RxA1—RECEIVE CARRIER (PINS 15, 16)

The receive carrier is the FSK input to the demodulator through the receive band-pass filter. RxA1 is the noninverting input and RxA2 is the inverting input of the receive hybrid (duplexer) operational amplifier.

$\overline{LB}$—ANALOG LOOPBACK (PIN 2)

When a high level is applied to this pin (SQT must be low), the analog loopback test is enabled. The analog loopback test connects the TxA pin to the RxA2 pin and the RxA1 to analog ground. In loopback, the demodulator frequencies are switched to the modulation frequencies for the selected mode. (See Tables 1 and 2 and Figures 4c and 4d.)

When $\overline{LB}$ is connected to analog ground (V_{AG}), the modulator generates an echo cancellation tone of 2100 Hz for MC145442 CCITT V.21 and 2225 Hz for MC145443 Bell 103 systems. For normal operation, this pin should be at a logic low level (V_{SS}).

The power-down mode is enabled when both $\overline{LB}$ and SQT are connected to a logic high level. (See Table 2.)

Table 2. Functional Table

MODE Pin 13	SQT Pin 14	$\overline{LB}$ Pin 2	Operating Mode
1	0	0	Originate Mode
0	0	0	Answer Mode
X	0	V_{AG} ($V_{DD}/2$)	Echo Tone
X	0	1	Analog Loopback
X	1	0	Squelch Mode
X	1	V_{AG} ($V_{DD}/2$)	Squelch Mode
X	1	1	Power Down

MODE—MODE (PIN 13)

This input selects the pair of transmit and receive frequencies used during modulation and demodulation. When a logic high level is placed on this input, originate (Bell) or channel 1 (CCITT) is selected. When a low level is placed on this input, answer (Bell) or channel 2 (CCITT) is selected. (See Tables 1 and 2 and Figure 4.)

CDT—CARRIER DETECT TIMING (PIN 4)

A capacitor on this pin to V_{SS} sets the amount of time the carrier must be present before $\overline{CD}$ goes low. (See Applications Information for the capacitor values.)

$\overline{CD}$—CARRIER DETECT OUTPUT (PIN 3)

This output is used to indicate when a carrier has been sensed by the carrier detect circuit. This output goes to a logic low level when a valid signal above the minimum threshold level (defined by CDA pin 7) is maintained on the input to the hybrid circuit longer than the response time (defined by CDT pin 4). This pin is held at the logic low level until the signal falls below the maximum threshold level for longer than the turn off time. (See Applications Information and Figure 5.)

CDA—CARRIER DETECT ADJUST (PIN 7)

An external voltage may be applied to this pin to adjust the carrier detect threshold. The threshold hysteresis is internally fixed at 3 dB. (See Applications Information.)

X_{out}, X_{in}—CRYSTAL OSCILLATOR (PINS 8, 9)

A crystal reference oscillator is formed when a 3.579 MHz crystal is connected between these two pins. X_{out} (pin 8) is the output of the oscillator circuit, and X_{in} (pin 9) is the input to the oscillator circuit. When using an external clock, apply the clock to the X_{in} (pin 9) pin and leave X_{out} (pin 8) open. An internal 10 mΩ resistor and internal capacitors, typically 10 pF on X_{in} and 16 pF on X_{out}, allow the crystal to be connected without any other external components. Printed circuit board layout should keep external stray capacitance to a minimum.

FB—FILTER BIAS (PIN 10)

This is the negative input to the ac amplifier. In normal operation, this pin is connected to analog ground through a 0.1 μF bypass capacitor in order to cancel the input offset voltage of the limiter. It has a nominal input impedance of 16 kΩ. (See Figure 3.)

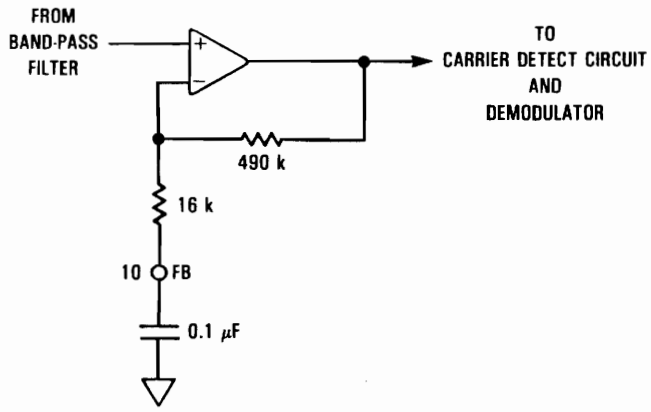


Figure 3. AC Amplifier Circuit

SQT—TRANSMIT SQUELCH (PIN 14)

When this input pin is at a logic high level, the modulator is disabled. The line driver remains active if $\overline{LB}$ is at a logic low level. (See Table 2.)

When both $\overline{LB}$ and SQT are connected to a logic high level, see Table 2, the entire chip is in a power down state and all circuitry except the crystal oscillator is disabled. Total power supply current decreases from 10 mA (maximum) to 300 μA (maximum).

GENERAL DESCRIPTION

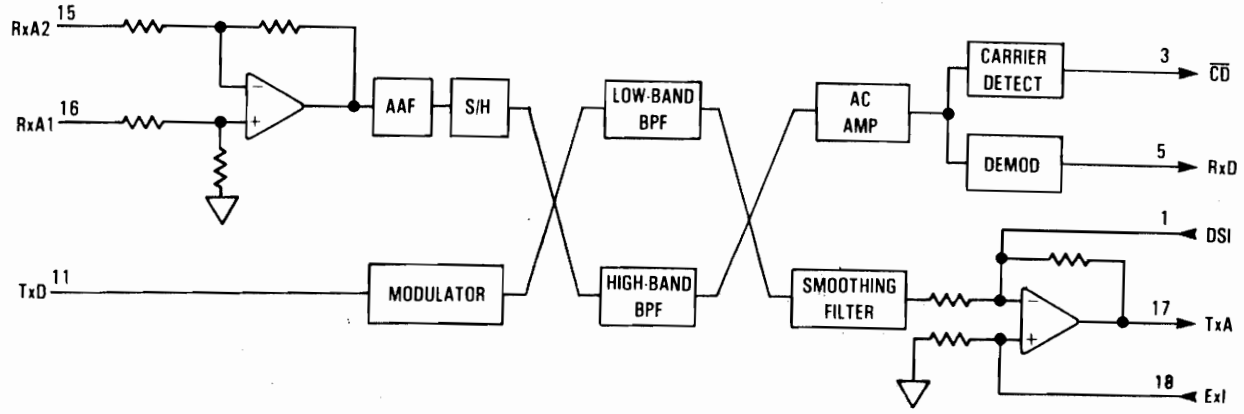
The MC145442 and MC145443 are full-duplex low-speed modems. They provide a 300 baud FSK signal for bidirectional data transmission over the telephone network. They can be operated in one of four basic configurations as determined by the state of MODE (pin 13) and $\overline{LB}$ (pin 2). The normal (non-loopback) and self test (loopback) modes in both answer and originate modes will be discussed.

For an originate or channel 1 mode, a logic high level is placed on MODE (pin 13) and a logic low level is placed on $\overline{LB}$ (pin 2). In this mode, transmit data is input on TxD, where it is converted to a FSK signal and routed through a low-band band-pass filter. The filtered output signal is then buffered by the Tx op-amp line driver, which is capable of driving −9 dBm onto a 600 Ω line. The receive signal is connected through a hybrid duplexer circuit on pins 15 and 16, RxA2 and RxA1. The signal then passes through the anti-aliasing filter, the sample-and-hold circuit, is switched into the high-band band-pass filter, and then switched into the ac amplifier circuit. The output of the ac amplifier circuit is routed to the demodulator circuit and demodulated. The resulting digital data is then output through RxD (pin 5). The carrier detect circuit receives its signal from the output of the ac amplifier circuit and goes low when the incoming signal is detected. (See Figure 4a.)

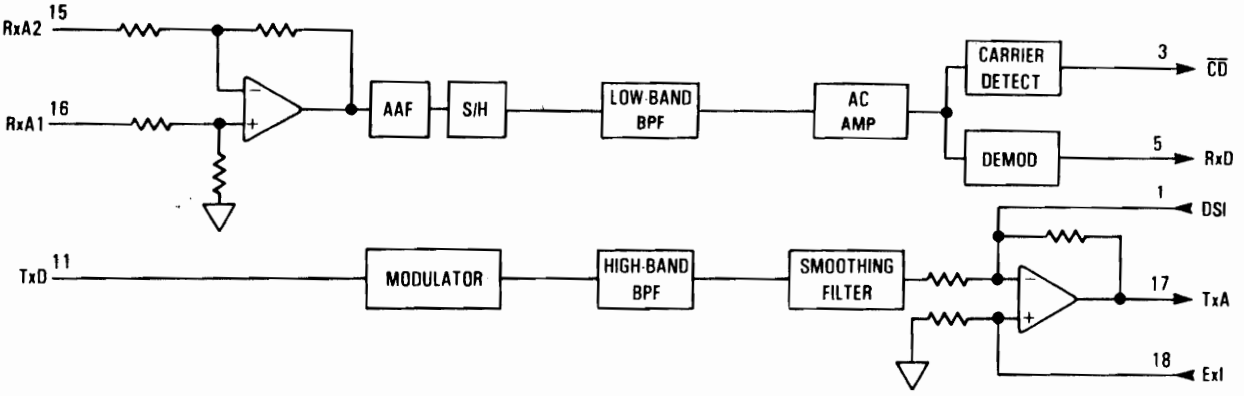
In the answer or channel 2 mode, a logic low level is placed on MODE (pin 13) and on $\overline{LB}$ (pin 2). In this mode, the data follows the same path except the FSK signal is routed to the high-band band-pass filter and the sample-and-hold signal is routed through the low-band band-pass filter. (See Figure 4b.)

In the analog loopback originate or channel 1 mode, a logic high level is placed on MODE (pin 13) and on $\overline{LB}$ (pin 2). This mode is used for a self check of the modulator, demodulator, and low-band pass-band filter circuit. The modulator side is configured exactly like the originate mode above except the line driver output (TxA pin 17) is switched to the negative input of the hybrid op-amp. The RxA2 input pin is open in this mode and the noninverting input of the hybrid circuit is connected to V_{AG}. The sample-and-hold output bypasses the filter so that the demodulator receives the modulated Tx data (see Figure 4c). This test checks all internal device components except the high-band band-pass filter which can be checked in the answer or channel 2 mode loopback test.

In the analog loopback answer or channel 2 mode, a logic low level is placed on MODE (pin 13) and a logic high level on $\overline{LB}$ (pin 2). This mode is used for a self check of the modulator, demodulator, and high-band pass-band filter circuit. This configuration is exactly like the originate loopback mode above, except the signal is routed through the high-band pass-band filter. (See Figure 4d.)

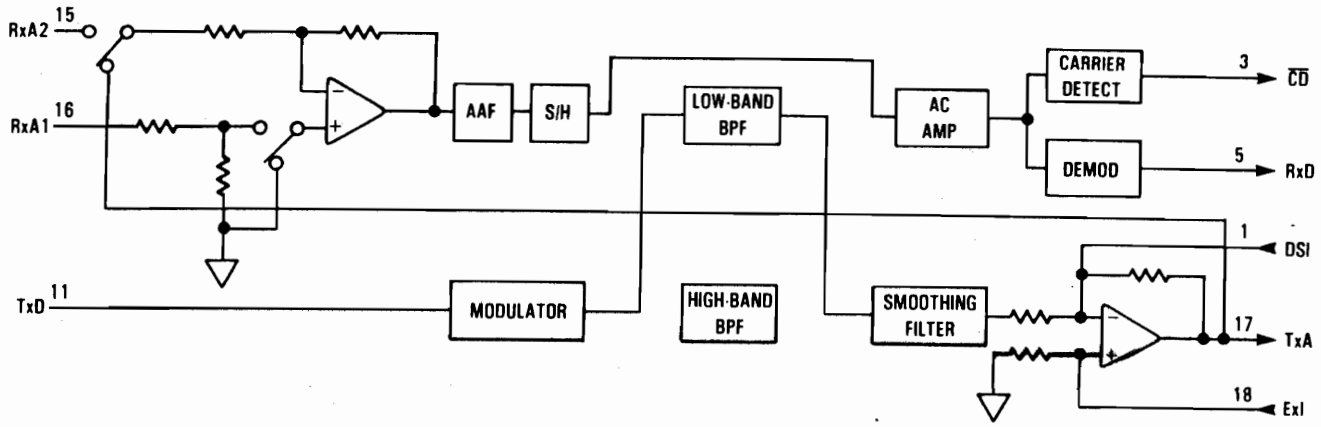


(a) ORIGINATE/CHANNEL 1 MODE (MODE = HIGH, $\overline{LB}$ = LOW)

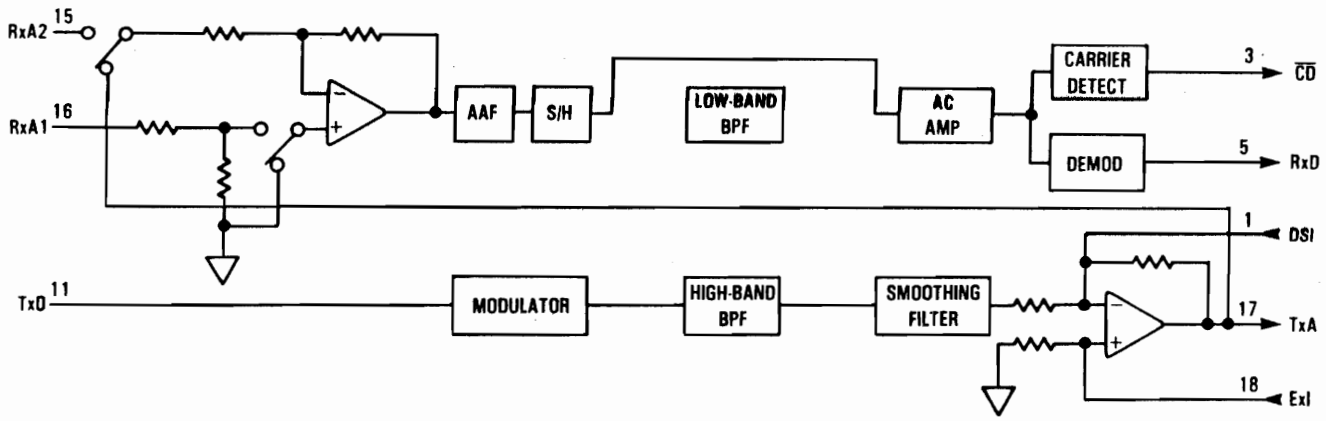


(b) ANSWER/CHANNEL 2 MODE (MODE = LOW, $\overline{LB}$ = LOW)

Figure 4. Basic Operating Modes



(c) ORIGINATE/CHANNEL 1 MODE AND ANALOG LOOPBACK STATE (MODE = HIGH, $\overline{LB}$ = HIGH)



(d) ANSWER/CHANNEL 2 MODE AND ANALOG LOOPBACK STATE (MODE = LOW, $\overline{LB}$ = HIGH)

Figure 4. Basic Operating Modes

APPLICATIONS INFORMATION

CARRIER DETECT TIMING ADJUSTMENT

The value of a capacitor, C_{CDT} at CDT (pin 4) determines how long a received modem signal must be present above the minimum threshold level before $\overline{CD}$ (pin 3) goes low. The C_{CDT} capacitor also determines how long the $\overline{CD}$ pin stays low after the received modem signal goes below the minimum threshold. The $\overline{CD}$ pin is used to distinguish a strong modem signal from random noise. The following equations show the relationship between t_{CDL}, the time in seconds required for $\overline{CD}$ to go low; t_{CDH}, the time in seconds required for $\overline{CD}$ to go high; and C_{CDT}, the capacitor value in μF.

Valid signal to $\overline{CD}$ response time: $t_{CDL} \approx 6.4 \times C_{CDT}$

Invalid signal to $\overline{CD}$ off time: $t_{CDH} \approx 0.54 \times C_{CDT}$

Example: $t_{CDL} \approx 6.4 \times 0.1\ \mu F \approx 0.64$ seconds

$t_{CDH} \approx 0.54 \times 0.1\ \mu F \approx 0.054$ seconds

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is set by internal resistors to activate $\overline{CD}$ with a typical -44 dBm (into 600 Ω) signal and deactivate $\overline{CD}$ with a typical -47 dBm signal applied to the input of the hybrid circuit. The carrier detect threshold level can be adjusted by applying an external voltage on CDA (pin 7). The following equations may be used to find the CDA voltage required for a given threshold voltage. (V_{on} and V_{off} are in volts RMS.)

$$V_{CDA} = 244 \times V_{on}$$

$$V_{CDA} = 345 \times V_{off}$$

Example (internally set)

$V_{on} = 4.9$ mV ≈ -44 dBm: $V_{CDA} = 244 \times 4.9$ mV $= 1.2$ V

$V_{off} = 3.5$ mV ≈ -47 dBm: $V_{CDA} = 345 \times 3.5$ mV $= 1.2$ V

Example (externally set):

$V_{on} = 7.7$ mV ≈ -40 dBm: $V_{CDA} = 244 \times 7.7$ mV $= 1.9$ V

$V_{off} = 5.4$ mV ≈ -43 dBm: $V_{CDA} = 345 \times 5.4$ mV $= 1.9$ V

The CDA pin has an approximate Thevenin equivalent voltage of 1.2 V and an output impedance of 100 kΩ. When using the internal 1.2 volt reference a 0.1 μF capacitor should be connected between this pin and V_{SS}. (See Figure 5.)

TRANSMIT LEVEL ADJUSTMENT

The power output at TxA (pin 17) is determined by the value of resistor R_{TLA} that is connected between TLA (pin 20) to V_{DD} (pin 6). Table 3 shows the R_{TLA} values and the corresponding power output for a 600 Ω load. The voltage at TxA is twice the value of that at ring and tip because TxA feeds the signal through a 600 Ω resistor R_{Tx} to a 600 Ω line transformer. (See Figure 7.) When choosing resistor R_{TLA}, keep in mind that -9 dBm is the maximum output level allowed from a modem onto the telephone line (in the U.S.). In addition, keep in mind that maximizing the power output from the modem optimizes the signal-to-noise ratio, improving accurate data transmission.

Table 3. Transmit Level Adjust

Output Transmit Level (Typical into 600 Ω)	R_{TLA}
−12 dBm	∞
−11 dBm	19.8 kΩ
−10 dBm	9.2 kΩ
−9 dBm	5.5 kΩ

THE LINE DRIVER

The line driver is a power amplifier used for driving the telephone line. Both the inverting and noninverting input to the line driver are available for transmitting externally generated tones.

ExI (pin 18) is the noninverting input to the line driver and gives a fixed gain of 2 ($R_i = 50$ kΩ). The average signal level must be the same as V_{AG} to maintain proper operation. This pin should be connected to V_{AG} if not used.

The driver summing input (DSI, pin 1) may be used to connect an external signal, such as a DTMF dialer, to the phone line. When applying a signal to the DSI pin, the modulator should be squelched by bringing SQT (pin 14) to a logic high level. DSI MUST be left OPEN if not used.

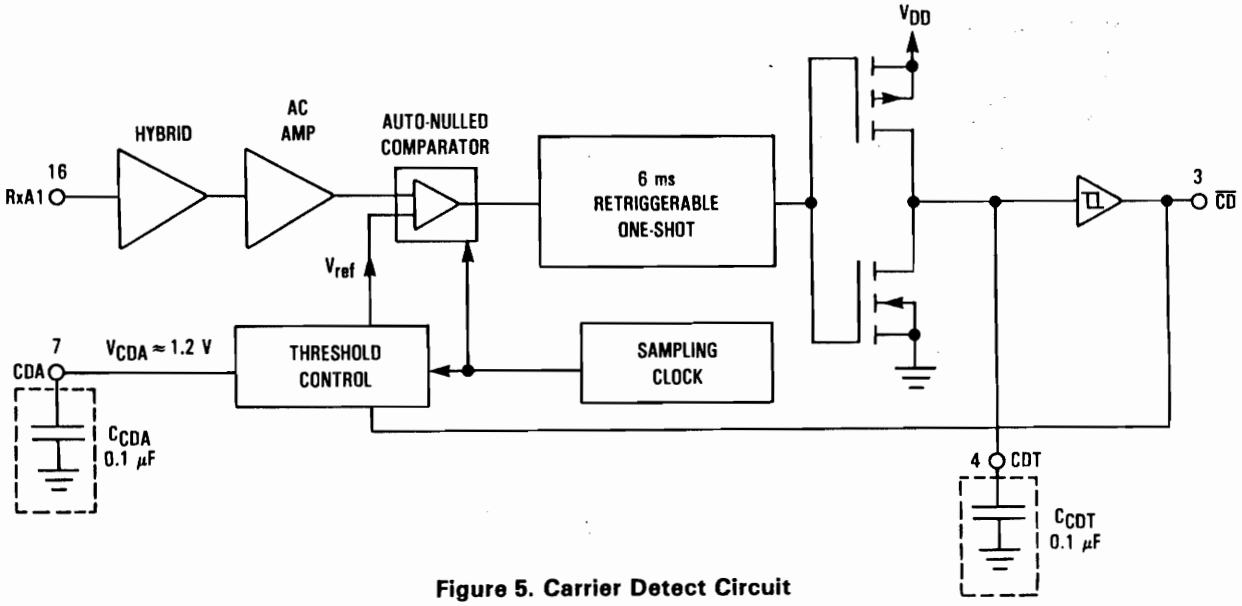


Figure 5. Carrier Detect Circuit

In addition, the DSI pin is the inverting side of the line driver and allows adjustable gain with a series resistor R_{DSI}. (See Figure 6.) The voltage gain, A_V, is determined by the equation:

$$A_V = -\frac{R_f}{R_{DSI}}$$

where $R_f \approx 20\ k\Omega$.

Example: A resistor value of 20 kΩ for R_{DSI} will provide unity gain.

$$A_V = -(20\ k\Omega/20\ k\Omega) = -1$$

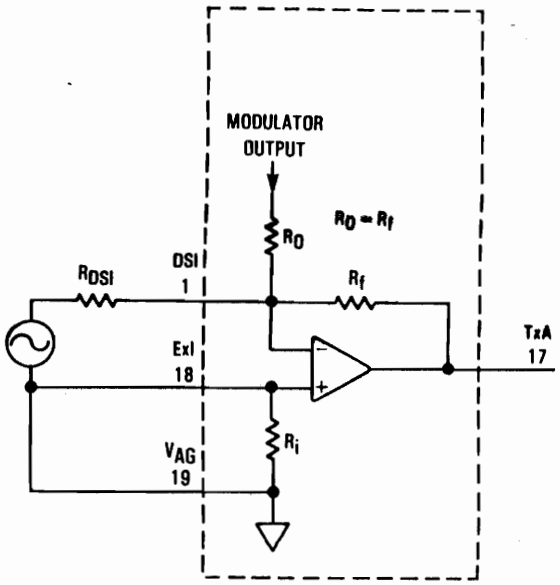
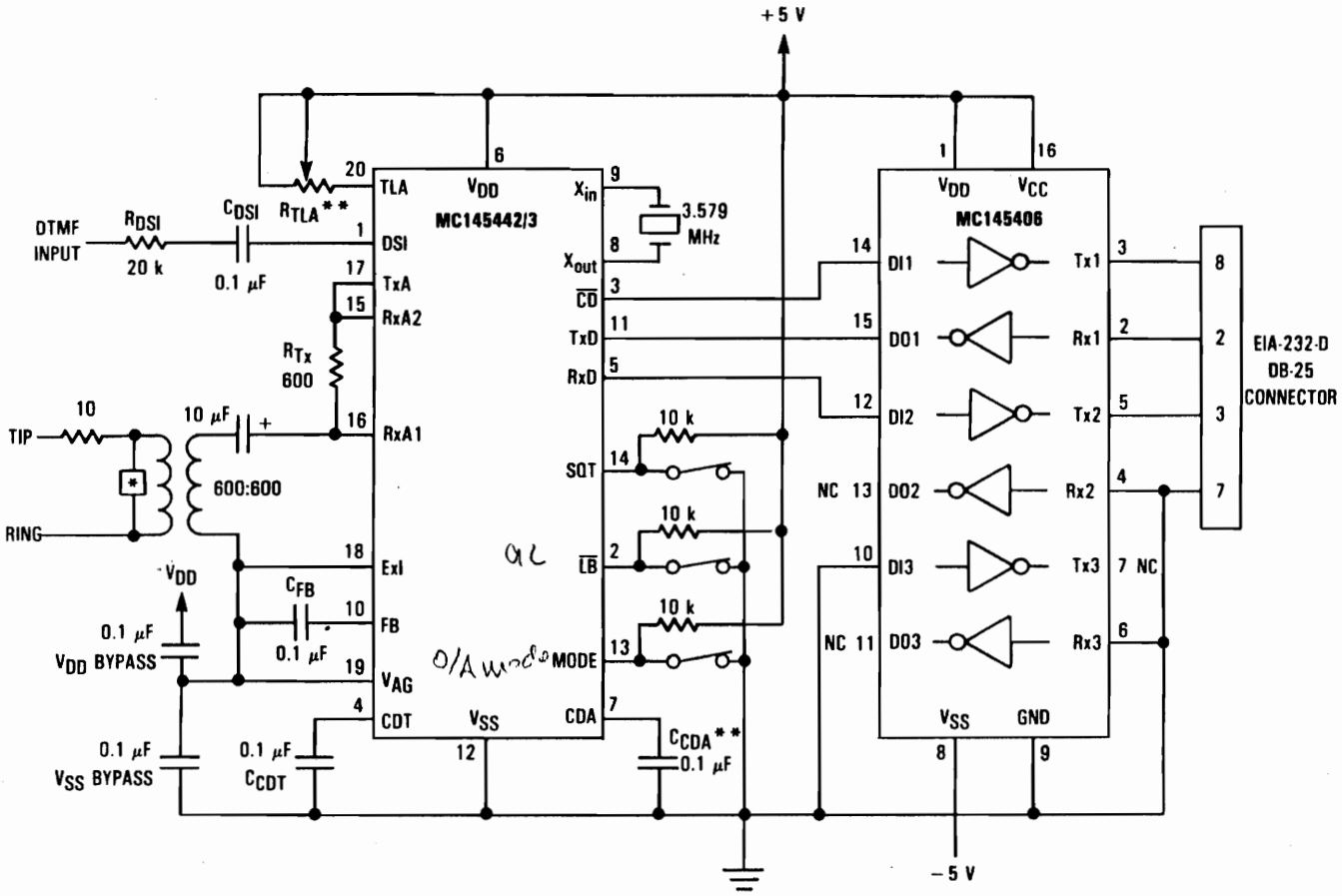


Figure 6. Line Driver Using the DSI Input



*Line protection circuit
**Refer to the applications information for values of C_{CDA} and R_{TLA}

Figure 7. Typical MC145442/MC145443 Applications Circuit

VIÐAUKI M

Diskettur með forritum

Fjölritunarstofa
Daníels Halldórssonar