ORKUSTOFNUN
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TENGIBÚNAÐUR FYRIR VERSATEK TEIKNARA

Sverrir Hákonarson

OS-90005/JHD-01 B Febrúar 1990

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Verknr. 533010

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1. INNGANGUR

Árið 1988 var keyptur á Orkustofnun Versatek teiknari og var tengdur við HP 9000 tölvu stofnunarinnar. Í ljós kom að teiknarinn var ekki fyllilega samhæfður tölvunni Því var smíðaður tengibúnaður til þess að leysa þessi vandamál í því sambandi og honum komið fyrir við hliðina á tölvunni.

2. TENGIBÚNAÐUR

Í tölvunni er sérstakt tengibretti til þess að stýra teiknaranum. Það er af tegundinni HP 2711A, asynchronous fifo interface (AFI). Ýtarlegar upplýsingar um það er að finna í viðauka. Frá tengibrettinu liggur 96 leiðara kapall samtals 48 mismunamerki (e. twisted pair). Af þeim eru 19 merki notuð fyrir teiknarann, 11 eru stýrimerki ásamt 8 gagnalínum. Þau eru talin upp í töflu 1.

VERSATEK		HP 27114A		
MERKI	NÚMER	NÚMER	MERKI	LITUR
IN1+	1	A01	SD0-	S AH
IN1-	20	C01	SD0+	S HA
IN2+	2	A03	SD1-	S GH
IN2-	21	C03	SD1+	S HG
IN3+	3	A05	SD2-	S BIH
IN3-	22	C05	SD2+	S HBI
IN4+	4	A07	SD3-	S BH
IN4-	23	C07	SD3+	S HB
IN5+	5	A09	SD4-	S GrH
IN5-	24	C09	SD4+	S HGr
IN6+	6	A11	SD5-	S AR
IN6-	25	C11	SD5+	S RA
IN7+	7	A13	SD6-	S GR
IN7-	26	C13	SD6+	S RG
IN8+	8	A15	SD7-	S BIR
IN8-	27	C15	SD7+	S RBI
CLEAR+	9	B30	CTL2-	S GrH
CLEAR-	28	A30	CTL2+	S HGr
PICLK+	10	A14	PCTL-	S AH
PICLK-	29	B14	PCTL+	S HA
READY+	11	B22	PFLG+	R GH
READY-	30	A22	PFLG-	R HG
PRINT+	12	A30	CTL2+	S HGr
PRINT-	31	B30	CTL2-	S GrH
GND	13			
ONLIN	32	A26	STS1+	R RG
SPP+	14	B30	CTL2-	S GrH
SPP-	33	A30	CTL2+	S HGr
RESET+	15	B30	CTL2-	S GrH
RESET-	34	A30	CTL2+	S HGr
RFFED+	16	A18	CTL1-	S BH
RFFED-	35	B18	CTL1+	S HB
REOTR+	17	B30	CTL2-	S GrH
REOTR-	36	A30	CTL2+	S HGr
RLTER+	18	B16	CTL0-	S BIH
RLTER-	37	A16	CTL0+	S HBI
NOPAP	19	A24	STS0+	R RA

TAFLA I Tengingar milli tölvunnar og teiknarans.

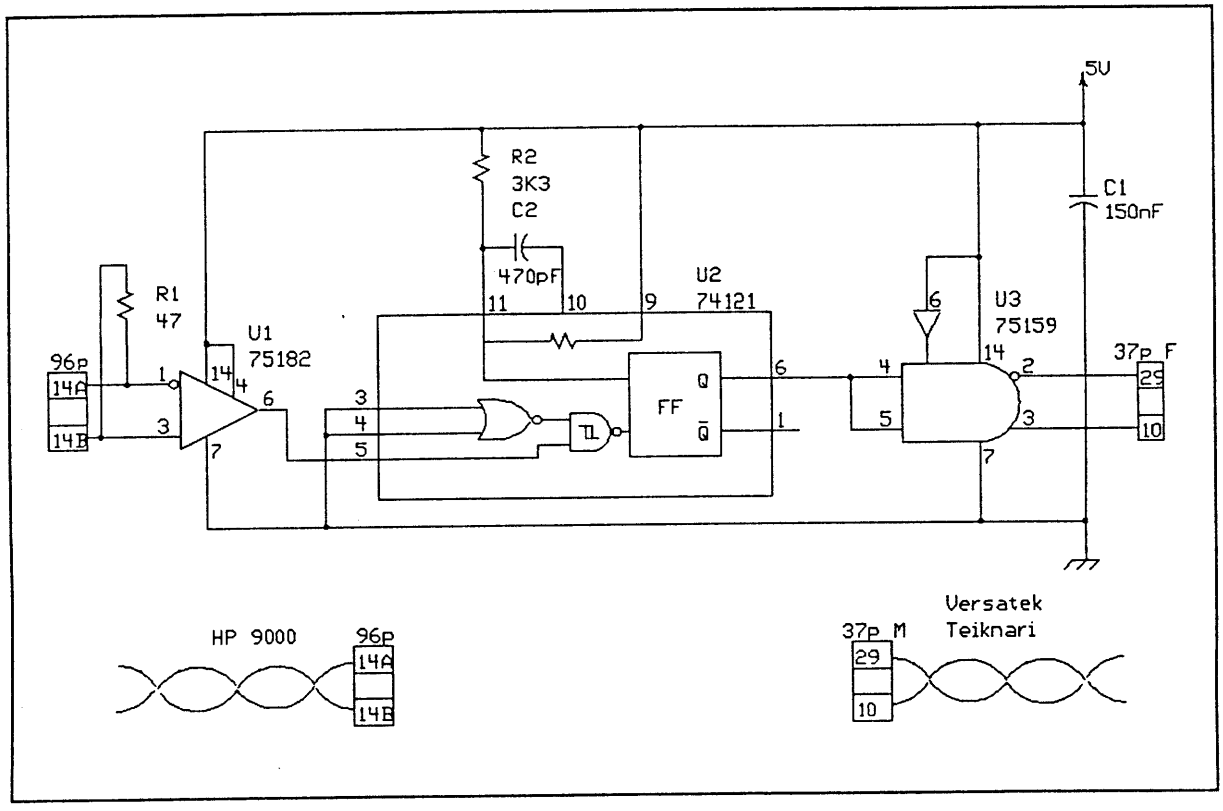
Tafla 2 skýrir út skamstafanir lita í töflu 1.

Eitt merkið, PCTL, frá tölvunni er notað sem klukkumerki og tengist PICLK á teiknaranum. Þetta merki er ekki forritanlegt og því er ekki hægt að stýra því að vild. Því reyndist nauðsynlegt að smíða rás sem gerði stuttan púls úr merkinu í hvert sinn sem það fer úr 0 í 1. Púlsinn þarf að vera um 1 μs að lengd. Önnur merki fara óbreytt á milli tölvunnar og teiknaranns samkvæmt töflu 1.

Skamst.	Litir:
H	Hvítt
A	Appelsínugult
G	Grænt
Bl	Blátt
R	Rautt
Gr	Grátt
B	Brúnt

TAFLA II Skammstafanir lita í töflu 1

3. RAFRÁSIN



MYND 1 Teikning af rásinni

Mynd 1 sýnir teikningu af rásinni. Hún byggir á 74121, "monostable multivibrator" rás. Við hana er tengdur þéttir C2 og viðnám R2. Stærð þéttisins og viðnámsins ákveður

lengd púlsins samkvæmt eftirfarandi formúlu.

$$T_w = R_2 C_2 \ln 2 \approx 0{,}7 R_2 C_2$$

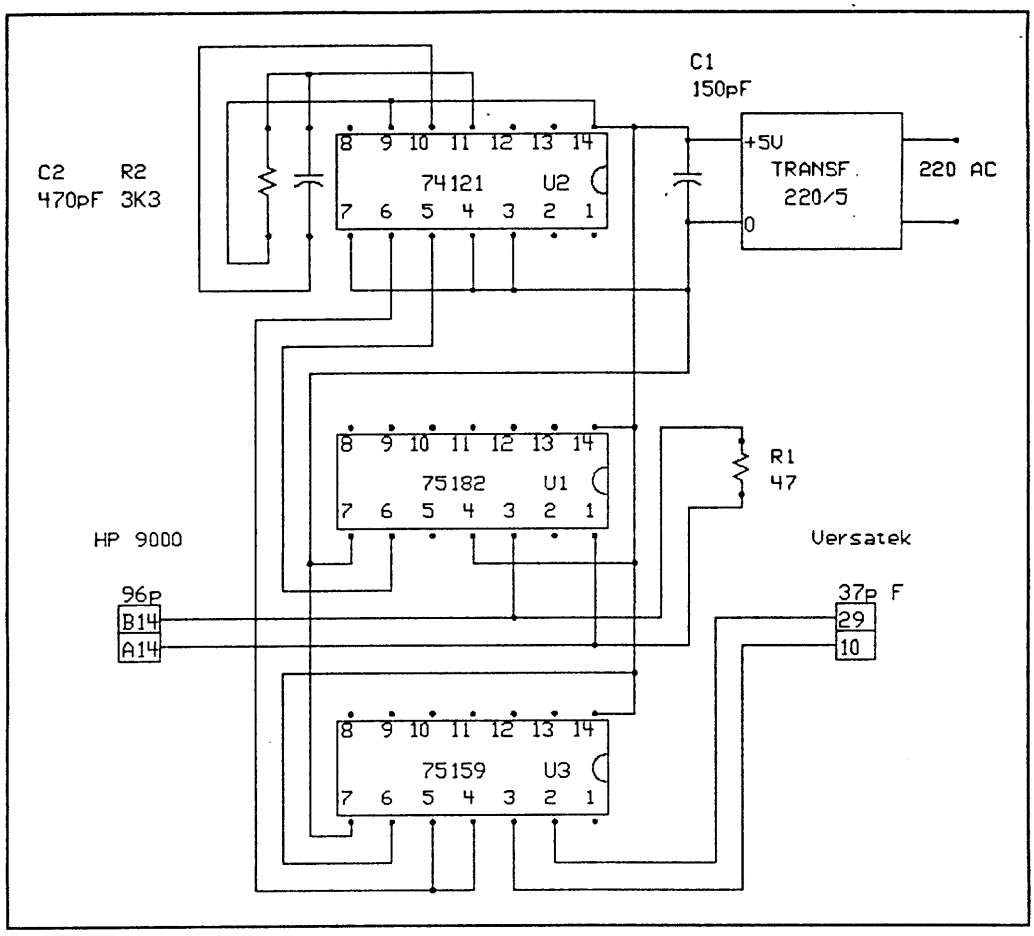
Nú þarf púlslengdin að vera u.þ.b. 1 μs, en 3,3 KΩ viðnám og 470 pF þéttir gefa einmitt þá niðurstöðu. Þessum gildum má auðveldlega breyta.

Þar sem merkið frá tölvunni er mismunamerki er notuð móttakararás U1, sem ræður við slíkt merki, og breytir því í TTL merki. Hún er af tegundinni 75184. Til þess að samhæfa viðnámið í kaplinum sem er 50 Ω, og viðnámið í móttakararásinni er sett 47 Ω viðnám R1, fyrir framan hana. Innmerkið er tengt við pinna 14A og 14B á 96 pinna tengi.

Á sama hátt tekur sendirásin U3, við TTL merki frá U2 og sendir það frá sér sem mismunamerki, sem tengt er við pinna 10 og 29 á 37 pinna kvennkyns D tengi. Sendirásin er af tegundinni 75159, en upplýsingar um hana ásamt upplýsingum um 75182 og 74121 er að finna í viðauka.

Afl fær rásin frá 220 Volta spennubreyti. Hann hefur innbyggðann afriðil ásamt reglunarrás. Spennan frá honum er 5 Volta jafnspenna.

Rásar íhlutirnir eru ekki lóðaðir á tengibrettið heldur eru notaðir sérstakir vírar sem eru vafðir um lappir þeirra, á ensku kallað wire wrap. Þessi tengiaðferð gerir það að verkum að auðvelt er að breyta rásinni og prófa fleirri tengimöguleika. Teikning af tengingum er á mynd 2.



MYND 2 Tengingar víra milli rása íhluta

VIÐAUKI A.

VERSATEK TEIKNARI

VERSATEC
A XEROX COMPANY

Electrostatic Printer/Plotter Interface Specification

INTRODUCTION

The basic interface is the standard signal connection point for all Versatec printers, plotters, and printer/plotters. This bulletin provides a detailed technical description of the interface for all Versatec 8½, 11, and 20-inch electrostatic units; pin connection lists and timing diagrams are also provided. The information given here does not pertain to special computer interfaces, data communication interfaces, software, or special input codes.

Specifications on all Versatec electrostatic units, Versatec controllers, and Versaplot plotting software systems are available from the Versatec Marketing Department in Santa Clara, California.

GENERAL

Electrostatic writing is accomplished by programming the voltage applied to a stationary linear array of writing nibs which produce an invisible charge directly on the surface of dielectrically-coated paper. The charge is developed by a liquid toner which produces a permanent, high contrast visible image of the data received as the paper moves out of the machine (Figure 1).

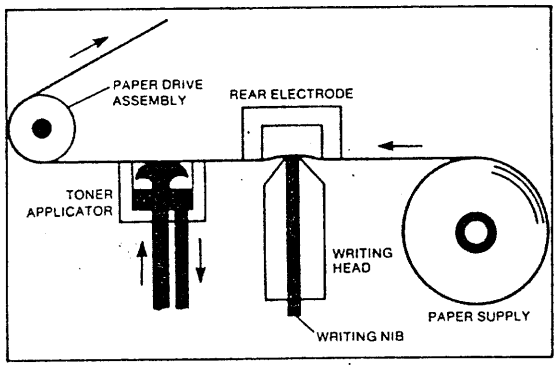


FIGURE 1. TYPICAL VERSATEC CONFIGURATION SHOWING PRINTER/PLOTTER OPERATION

Versatec printers accept asynchronous USASCII data in serial or parallel format. The ASCII input is decoded and converted to characters by means of a Read Only Memory (ROM) which is included in the standard configuration. Versatec plotters accept software-generated unweighted binary data in eight-bit bytes for raster scan plotting of graphic information. Each data bit relates to one nib in the plotting mode. Combination printer/plotters accept both printing and plotting input data.

Standard Versatec printers, plotters, and printer/plotters are supplied with both parallel and serial signal interfaces. The parallel interface accepts data in a bit parallel, character, or byte parallel mode. The serial interface accepts data in a bit serial, character, or byte serial mode.

PRINT OPERATIONS

Print operations are applicable to all Versatec printers and printer/plotters. Print data may be applied at either the parallel signal interface at connector J1, or the serial signal interface at connector J2 (see pin assignments, Figures 2 and 3). The PRINT input signal, applied at pin 12, J1, parallel signal interface, controls selection of PRINT or PLOT mode. When PRINT is HIGH and input clock, PICLK, is received, PRINT mode is selected. When PRINT is LOW and input clock, PICLK, is received, PLOT mode is selected. On printers or plotters only, this line is internally fixed to select the appropriate mode. The PRINT line can only be changed when the Versatec unit is ready.

The print input accepts ASCII seven or eight-level code in parallel or serial form. The selection of serial or parallel input may be made by logical selection at parallel input connector, J1, pin 13. This signal line, PARIN, must be held LOW for serial input or HIGH for parallel input. An open connection is interpreted as a HIGH.

The character generator in the Versatec printer contains a ROM which stores up to 256 characters. Characters are entered and stored in a line buffer. When the buffer is full (one line of characters) the line is automatically printed. If the buffer contains less than a full line of characters, a control command is required to initiate printing.

Control commands may be transmitted using the remote control lines described in Figure 4, or by transmitting the appropriate ASCII control code as shown in Figure 5. There are no ASCII control codes when the 128-character or larger set is used.

Automatic hardware line counting is provided for use with fan-fold paper. This feature provides automatic page separation and prevents printing on the perforated folds. When the page is full the paper will automatically advance to top of form. The line counter is reset by the form feed (FF), end of transmission (EOT), or reset control signals, as well as by entering the PLOT mode. Automatic line counting is disabled when operation with roll paper is selected via the ROLL/FAN-FOLD control switch, or when in the PLOT mode.

PLOT OPERATIONS

Plot operations are applicable to all Versatec plotters and printer/plotters. Plot input data are applied at the parallel interface at connector J1, or the serial interface at connector J2 shown in Figures 6 and 7, respectively.

Data consist of eight-bit binary unweighted bytes. For the number of bits per complete raster scan, refer to Table 1 on page 4.

J1 – Parallel input. Connector type: Cannon DCC-37P; Mating connector: Cannon DCC-37S. Twisted pairs not to exceed 50 feet.

	SIGNAL NAME	SIGNAL PIN NO.	SIGNAL COMMON PIN NO.	PAIR NO.	MNEMONICS
(Highest # Nib)	Input Bit 1 (LSB)	1	20	1	IN01
	Input Bit 2	2	21	2	IN02
	Input Bit 3	3	22	3	IN03
	Input Bit 4	4	23	4	IN04
	Input Bit 5	5	24	5	IN05
	Input Bit 6	6	25	6	IN06
	Input Bit 7	7	26	7	IN07
(Lowest # Nib)	Input Bit 8 (MSB)	8	27	8	IN08
	Clear	9	28	9	$\overline{\text{CLEAR}}$
	Parallel Input Clock	10	29	10	PICLK
	Ready	11	30	11	$\overline{\text{READY}}$
	Printer	12	31*	12	PRINT
	Parallel	13	31*	13	PARIN
	Simultaneous Print/Plot	14	33	14	$\overline{\text{SPP}}$
	Remote Reset	15	34	15	$\overline{\text{RESET}}$
	Remote Form Feed	16	35	16	$\overline{\text{RFFED}}$
	Remote End of Transmission	17	36	17	$\overline{\text{REOTR}}$
	Remote Line Terminate	18	37	18	$\overline{\text{RLTER}}$
	No Paper Sense	19**		19	NOPAP
	On-Line	32**			$\overline{\text{ONLIN}}$

*Two commons tied to pin 31 **No common for these two signals.

NOTE: There is no ground return provided for long line drivers and receivers.

FIGURE 2. PARALLEL SIGNAL INTERFACE CONNECTOR PIN ASSIGNMENTS

J2–Serial input. Connector type: Cannon DBC-25S; Mating connector: Cannon DBC-25P.

PIN	FUNCTION		REMARKS
	USED	NOT USED BUT TERMINATED	
1*	Protective Ground		Ground
2		Transmitted Data	Held At Mark
3	Received Data		Serial Data Input
4		Request To Send	Held At Mark
5		Clear To Send	Terminated To GND
6		Data Set Ready	Terminated To GND
7*	Signal Ground		Signal Common
8		Received Line Signal	Terminated To GND
12		Sec. Received Line Sig. Detect.	Terminated To GND
13		Sec. Clear To Send	Held At Mark
14		Sec. Transmitted Data	Held At Mark
15		DCE Source	Terminated To GND
19		Sec. Request To Send	Held At Mark
20		Data Terminal Ready	Held At Space
21		Sig. Quality Detect.	Terminated To GND
22		Ring Indicator	Terminated To GND
25**	Ready ($\overline{\text{SERDY}}$)		Serial Ready

*Pins 1 and 7 are connected internally

**Logic Level on Ready ($\overline{\text{SERDY}}$) is: High = +3.5V to 5V = BUSY
Low = –0.5V to +0.5V = READY

FIGURE 3. SERIAL SIGNAL INTERFACE CONNECTOR PIN ASSIGNMENTS

Remote control signals are used to control electrostatic unit operations. They apply to PRINT, PLOT, and SPP operations and facilitate remote control of a Versatec unit by a computer or other device.

SIGNAL NAME	SIGNAL MNEMONIC	SIGNAL REQUIRED	OPERATION
Clear	$\overline{\text{CLEAR}}$	Low Going Pulse, 300ns Min.	a. Clears Buffer when Matrix is in Data Entry Mode (when $\overline{\text{READY}}$ is LOW). b. Causes $\overline{\text{READY}}$ to go HIGH for 25 μs or less.
Remote Reset	$\overline{\text{RESET}}$	Low Going Pulse, 300ns Min.	a. Clears Buffer and initializes all logic. b. Causes $\overline{\text{READY}}$ to go HIGH for 25 μs or less. c. Will not reset out of paper.
Remote Line Terminate	$\overline{\text{RLTER}}$	Low Going Pulse, 300ns Min.	a. Forces Write Cycle. b. Causes $\overline{\text{READY}}$ to go HIGH for duration of write cycle. c. If in plot mode first $\overline{\text{RLTER}}$ after full buffer is ignored.
Remote Form Feed**	$\overline{\text{RFFED}}$	Low Going Pulse, 300ns Min.	a. Forces Write Cycle. b. With Fan-Fold Operation causes paper to advance to top of next page. c. With Roll Operation causes paper to advance approximately 2.5 inches. d. Causes $\overline{\text{READY}}$ to go HIGH until paper is advanced.
Remote End of Transmission*	$\overline{\text{REOTR}}$	Low Going Pulse, 300ns Min.	a. Forces Write Cycle. b. With Fan-Fold Operation causes paper to advance 8 inches, then to top of next page. c. With Roll Operation causes paper to advance approximately 8 inches. d. Causes $\overline{\text{READY}}$ to go HIGH until paper is advanced.

*Not to be asserted when in SPP and PRINT mode.
**If FF is issued while in fan-fold mode and unit is switched to ROLL, the Versatec unit will go out of paper.

FIGURE 4. REMOTE CONTROL SIGNALS

CONTROL SIGNAL NAME	ASCII CODE (OCTAL)	OPERATION		
EOT (End of Transmission)	004	Causes print cycle and paper advance of 8 inches, then stop if in roll mode, or continue advance to top of next page if in fan-fold mode. Do not use if in SPP mode.		
FF (Form Feed)	014	Causes print cycle and paper advance of 2-1/2 inches if in roll mode, or advance to top of next page if in fan-fold mode. Do not use if in SPP mode.		
LF (Line Feed)	012	Causes print cycle and paper advance of one line except when: 1. Follows print of a full buffer. 2. Follows a Carriage Return which causes a print cycle.		
CR (Carriage Return)	015	Causes print cycle and paper advance of one line, only if buffer has at least one character entered but is not full.		
DC1	021	When in serial mode, changes from print to plot mode for one scan.		
CR, LF	015, 012	FB* IGNORED, IGNORED	PB* WRITE, IGNORE	EB* IGNORE, WRITE

FIGURE 5. ASCII CONTROL CODES

*FB = Full Buffer; PB = Partial Buffer; EB = Empty Buffer.

Each dot corresponds to a single bit in the buffer. If a bit is "1", a black dot is plotted at the point corresponding to the bit position in the buffer. Input bit 8 (IN08) is the MSB and corresponds to the lowest numbered writing nib in each byte. For example, in the first byte transmitted, IN08 should address the first nib. Thus, IN01 of the last byte would address the last nib on the Versatec unit.

When the last byte is stored in the buffer, a single scan is automatically generated and one scan line of data points is plotted. A paper increment equal to the horizontal resolution is generated and the Versatec unit is then ready to plot another scan line of data points. Remote control signals are described in Figure 4.

($\overline{\text{RLTER}}$, $\overline{\text{RFFED}}$, $\overline{\text{REOTR}}$,) may be used to generate the scan if less than a full buffer is entered. The clear line ($\overline{\text{CLEAR}}$) may be used to clear the buffer prior to entering data.

Data may be entered (when $\overline{\text{READY}}$ is LOW) up to the maximum rate of 1 million bytes per second.

SIMULTANEOUS PRINT/PLOT (SPP) OPERATIONS

Simultaneous Print/Plot (SPP) operation is provided to permit direct overlaying of character data generated by the

internal character generator, with plotting data generated on a dot basis. This is an optional feature on some Versatec printer/plotters.

Printing and plotting data are entered in parallel format to input J1 from a computer or other data source. The internal character generator generates the appropriate character format from the input ASCII code.

Plotting data are entered as unweighted binary eight-bit bytes as described under Plot Operations.

When the plot buffer is filled or an $\overline{\text{RLTER}}$ is given, the plot buffer is scanned and a single row of dots which corresponds to the binary contents of the plot buffer is written.

During the scanning process, the print buffer is likewise scanned. The corresponding dot(s) of each character are OR'D with the plot buffer output, thus overlaying the printed and plotted data. NOTE: On Model 200A the printing buffer holds 70 characters maximum during SPP operation (see Table 1 below).

TABLE 1. MAXIMUM BUFFER LENGTH

Model	Print		Plot	
	Characters/ line	No. of scans 64/96, 128*	Bits	Bytes
200A	80 (70 SPP)	8/10	560	70
800	100	10/12	800	100
900	100	20/20	1600	200
1100	132	10/12	1024	128
1200	132	20/20	2112	264
1600	100	20/20	1600	200
2000	232	10/12	1856	232
2030	232	10/12	1856	232
2160	180	20/20	2880	360

The SPP mode is controlled by a single input line, $\overline{\text{SPP}}$. When $\overline{\text{SPP}}$ is LOW, only parallel data bytes are accepted and the Versatec unit operates only in the SPP mode.

If the PRINT control line is LOW, the data byte is stored in the plot buffer. If PRINT is HIGH the data byte is stored in the print buffer. Remote or ASCII control codes, EOT (End of Transmission), or FF (Form Feed) are illegal codes in the SPP mode when the PRINT control line is HIGH. When the PRINT control line is LOW, i.e., in PLOT mode, the remote control line, $\overline{\text{REOTR}}$, functions as described in Figure 4.

*NOTE: The number of scans value listed is the minimum value for standard characters. A maximum of 32 scans may be required for oversized and special characters.

Normal operation consists of first filling the print buffer. This is accomplished by placing the PRINT line HIGH, in the SPP mode, and entering characters. If the buffer is not filled, the line may be terminated by a CR or LF code. The $\overline{\text{READY}}$ line now goes to the busy state, indicating that the buffer is full. The PRINT line is now placed LOW, indicating PLOT mode. This causes the $\overline{\text{READY}}$ line to go LOW indicating the plot buffer can be filled. Unweighted binary plot data are now loaded into the plot buffer, one byte at a time, until the plot buffer is full or an $\overline{\text{RLTER}}$ is given. The $\overline{\text{READY}}$ line now goes busy again and a single scan is generated. Note that the writing process is controlled by the plot buffer. An input clock is required when changing from PRINT to PLOT.

To completely print the line in the print buffer, a number of scans must be plotted. New data can be entered into the print buffer after the last scan of the previous line of characters is completed.

Operation of the Control Lines in the SPP mode is as shown in Table 2.

SPP OPTION FOR 1100A, 96/128-CHARACTER SET

In the SPP mode the Versatec unit becomes a raster scan plotter with a hardware-generated print capability. That is, a write cycle can only be caused by terminating the plot buffer which will generate one scan. ASCII-generated Form Feed (FF) and End of Transmission (EOT) characters will not be honored.

For example, in the following routine we will overlay the print character "A" and a diagonal line plotted left to right and examine it step by step:

Step 1. Set Print

Step 2. Set SPP

TABLE 2. CONTROL LINE OPERATION, SPP MODE

SIGNAL NAME	SIGNAL LEVEL	OPERATION
PRINT	HIGH	Causes parallel data bytes to be loaded into print buffer. $\overline{\text{READY}}$ indicates status of print buffer.
	LOW	Causes parallel data bytes to be loaded into plot buffer. $\overline{\text{READY}}$ indicates status of plot buffer.
$\overline{\text{SPP}}$	HIGH	Normal machine operation.
	LOW	SPP mode, parallel data only.
$\overline{\text{CLEAR}}$	Negative Going Pulse 300 ns Min.	Clears plot buffer (plot mode) or print buffer (print mode).
$\overline{\text{RESET}}$	Negative Going Pulse 300 ns Min.	Clears both print and plot buffer, resets all logic

Step 3. Send the following ASCII data:

SPACE	SPACE	"A"	Line Feed
$(040)_8$	$(040)_8$	$(101)_8$	$(012)_8$

Step 4. Set Plot

Step 5. Send the following Plot data (MSB=Bit 8)

$(200)_8$	$(000)_8$	LTER	=	Scan 1
$(100)_8$	$(000)_8$	LTER	=	Scan 2
$(040)_8$	$(000)_8$	LTER	=	Scan 3
$(020)_8$	$(000)_8$	LTER	=	Scan 4
$(010)_8$	$(000)_8$	LTER	=	Scan 5
$(004)_8$	$(000)_8$	LTER	=	Scan 6
$(002)_8$	$(000)_8$	LTER	=	Scan 7
$(001)_8$	$(000)_8$	LTER	=	Scan 8
$(000)_8$	$(200)_8$	LTER	=	Scan 9
$(000)_8$	$(100)_8$	LTER	=	Scan 10
$(000)_8$	$(040)_8$	LTER	=	Scan 11
$(000)_8$	$(020)_8$	LTER	=	Scan 12

Step 1 and 2
As far as the Versatec unit is concerned, it isn't necessary to be in the PRINT mode to set SPP. However, this is the sequence that must be followed with many of our controllers.

Once SPP is set it isn't necessary to switch in and out of SPP mode unless you wish to use the unit as a printer only.

Step 3
There is a two-space character prior to the "A" because the Plot width is four bytes narrower and centered with respect to Print.

When the print buffer is terminated (ASCII LF or CR or RLTER) or filled (132 print bytes) $\overline{\text{READY}}$ will indicate busy until the print buffer is cleared, the unit is reset, or the print cycle has been completed.

The function of the READY line is to indicate the status of the buffer being selected. Since the print buffer has been terminated and has not completed writing its contents, $\overline{\text{READY}}$ will indicate busy as long as Print is set (indicating the print buffer is not ready to receive data).

Step 4
When Plot is set, $\overline{\text{READY}}$ will go true (indicating the plot buffer is ready to receive data).

Step 5
Each time the plot buffer is terminated or filled, the Versatec unit will indicate busy until is has plotted the contents of the plot buffer and OR'D with the contents of the print buffer as decoded by the character generator for that particular scan.

After generating 12 plot scans, the print buffer will have completed the writing cycle and may again be selected.

PARALLEL SIGNAL INTERFACE

The parallel signal interface is used to receive parallel input data and control signals. It is used whenever high speed data transfer is required, as with a standard computer I/O data bus.

The parallel signal interface consists of eight data lines and 12 control lines. Figure 2 lists the connector pin assignments. Positive logic, TTL or DTL-compatible levels are used.

The ready line ($\overline{\text{READY}}$) indicates the current status of the Versatec unit. The unit is busy when $\overline{\text{READY}}$ is HIGH. Figure 6 shows the normal operation of the ready line during receipt of data. $\overline{\text{READY}}$ remains at the busy level for longer intervals while the Versatec unit is printing or plotting.

Data are accepted on eight lines (IN01-IN08). Data can only be entered when $\overline{\text{READY}}$ is LOW. Data consist of character codes or control codes as defined in Figure 8, Versatec ASCII Character Set, and Figure 5, ASCII Control Codes.

A parallel input clock pulse (PICLK) is required for each byte of input data. Figure 6 shows the timing relationship between the clock and the data signal. Clock pulses should be transmitted when $\overline{\text{READY}}$ is LOW. The maximum data transfer rate is 1 million eight-bit bytes per second.

The signal level on the printer line (PRINT) determines, in the case of printer/plotters only, whether the Versatec unit functions as a printer or a plotter. If PRINT is HIGH the unit functions as a PRINTER. An open line will be interpreted as a HIGH. If PRINT is LOW the unit functions as a plotter. For printer only or plotter only, the mode is determined internally.

Printer/plotters will write the data on paper in the mode last set (i.e., if "N" ASCII characters were entered into the buffer in the PRINT mode and the mode was then changed to PLOT and if the remainder of the buffer was filled with plot data or a RLTER or REOTR was issued, the entire buffer will be plotted rather than printed).

The signal level on the on-line ($\overline{\text{ONLIN}}$) is LOW when the Versatec unit power is on. A tie-up resistor must be provided by the user on this line to maintain a HIGH level when power is off, or the input cable is disconnected.

The no paper sense line (NOPAP) is HIGH if the paper supply is depleted. The red warning indicator, PAPER, on the control panel also lights to indicate the out-of-paper condition. A tie-up resistor must be provided by the user on this line to maintain a HIGH level when power is off, or the input cable is disconnected.

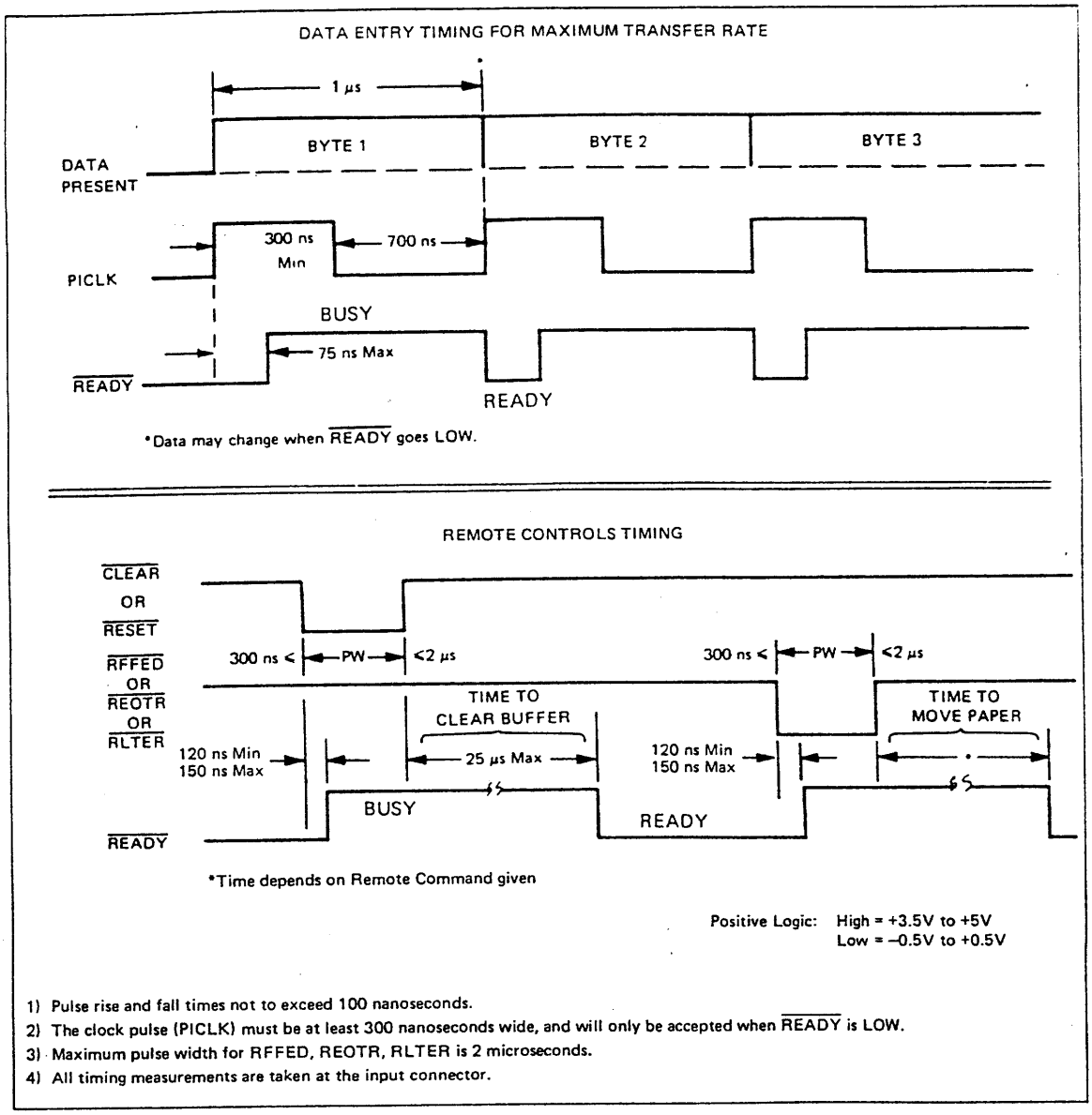
The simultaneous print/plot line ($\overline{\text{SPP}}$) is HIGH in normal operation. When LOW, SPP operation is indicated and only parallel data are accepted. The print line determines whether data bytes will be loaded into the print or plot buffer (SPP machines only). If the SPP option is not provided, this line is inoperative.

Operation of additional remote control lines is described in Figure 4.

SERIAL SIGNAL INTERFACE

The serial signal interface is used to receive asynchronous serial data. Either printing or plotting data may be received.

The serial signal interface may receive data if the input control line, PARIN, on J1, pin 13 (parallel signal interface) is LOW. This may be accomplished by using the supplied 37-pin parallel connector with pins 10 (PICLK) and 13 (PARIN) tied to pin 31 (GND). The serial signal interface



1) Pulse rise and fall times not to exceed 100 nanoseconds.
2) The clock pulse (PICLK) must be at least 300 nanoseconds wide, and will only be accepted when $\overline{\text{READY}}$ is LOW.
3) Maximum pulse width for RFFED, REOTR, RLTER is 2 microseconds.
4) All timing measurements are taken at the input connector.

FIGURE 6. PARALLEL SIGNAL INTERFACE

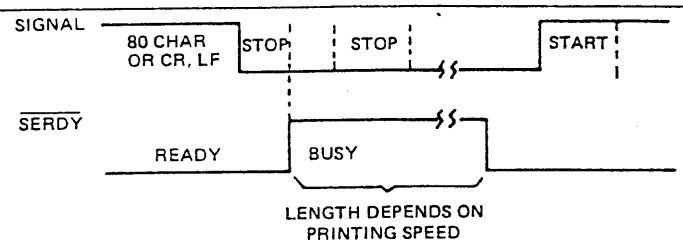
consists of two signal lines and a ready line. The remaining 13 RS 232C control lines are not used but are terminated in the Versatec unit.

The received data line is the input line for level shift, bit serial, character or byte serial data. The signal ground line is the data return line. All lines except serial ready ($\overline{\text{SERDY}}$) are negative logic, Teletype-compatible levels as described in Figure 3. If specified at time of order, positive logic, TTL-compatible levels may be supplied for all lines.

Pin assignments and negative logic voltage levels are compatible with EIA Standard RS232C.

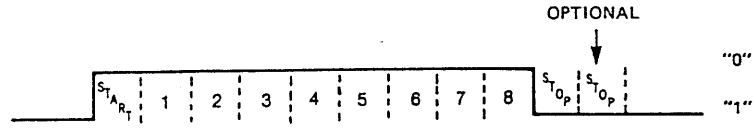
A serial ready line ($\overline{\text{SERDY}}$) is provided and it is recommended that data be entered only when $\overline{\text{SERDY}}$ is LOW. Data entered when $\overline{\text{SERDY}}$ is HIGH are lost. $\overline{\text{SERDY}}$ goes HIGH upon receipt of a full buffer on a Carriage Return (CR) or Line Feed (LF) code. Timing is shown in Figure 7. $\overline{\text{SERDY}}$ is connected to a normally unassigned pin on the EIA RS232C standard interface and the voltage levels are +5 volts for HIGH and 0 volts for LOW.

In single buffer units, data cannot be received while the machine is printing or plotting. After receipt of a LF or CR or a full buffer, the data transmitting source must not transmit while the Versatec unit is printing or plotting. In addition, for both single buffer and dual buffer Versatec models, a waiting time of approximately 2 seconds must be observed for the first print line or plot scan to allow toner to reach the toner channel. If no printing or plotting occurs for a period of 1.5 seconds or more, this waiting time must again be observed by the transmitting data source.



NOTE:

1) Positive or negative logic should be specified at time of order. Negative logic is supplied unless otherwise specified.
2) Signal positions 1-8 (see timing diagram) contain bits 1-8. Bit 1 is the LSB (least significant bit). Bit 8 is the MSB (most significant bit).
3) The second stop position is optional. Either 10 or 11 element codes are acceptable.



BIT ASSIGNMENT – SERIAL ASCII

STANDARD

Negative BI POLAR Logic
"1" (true) = –5V to –25V (MARK)
"0" (false) = +5V to +25V (SPACE)

OPTIONS

Positive BI POLAR Logic
"0" (true) = –5V to –25V (MARK)
"1" (false) = +5V to +25V (SPACE)

Positive TTL Logic
"1" (true) = +3.5V to +5V (+5V nominal)
"0" (false) = –0.5V to +0.5V (0V nominal)

FIGURE 7. SERIAL SIGNAL INTERFACE DATA ENTRY TIMING

The characters shown below are standard for Versatec models: LP-810, LP-960, LP-1150, LP-1175, LP-1616, LP-1250, 2000A and 2030A. There are four character variations for models LP-960, LP-1616 and LP-1250. These variations are given on the right side of the four boxes which contain two different characters.

BIT 4	BIT 3	BIT 2	BIT 1	BIT 7	0	0	0	0	0	0	1	1	1	1
				BIT 6	0	0	0	0	1	1	0	0	1	1
				BIT 5	0	1	0	1	0	1	0	1	0	1
0	0	0	0		+	α		•	SPACE	Ø	@	P	◣	p
0	0	0	1		±	DCL		DCL	!	1	A	Q	a	q
0	0	1	0		×	β		•	"	2	B	R	b	r
0	0	1	1		≠	γ		•	#	3	C	S	c	s
0	1	0	0		EOT	Δ	EOT	•	$	4	D	T	d	t
0	1	0	1		≡	ε		•	%	5	E	U	e	u
0	1	1	0		∞	θ		•	&	6	F	V	f	v
0	1	1	1		∈	λ		•	'	7	G	W	g	w
1	0	0	0		≤	μ		•	(	8	H	X	h	x
1	0	0	1		≥	ν		•	)	9	I	Y	i	y
1	0	1	0		LF	π	LF	•	*	:	J	Z	j	z
1	0	1	1		°	ρ		•	+	;	K	[	k	{
1	1	0	0		FF	Σ	FF	•	,	<	L	\	l	¦ |
1	1	0	1		CR	σ	CR	•	–	=	M	]	m	}
1	1	1	0		′	φ		•	.	>	N	↑ ^	n	~
1	1	1	1		″	ψ		•	/	?	O	← _	o	▪

124 SCIENTIFIC CHARACTER SET (OPTIONAL) **

64 CHARACTER SET

96 CHARACTER SET (OPTIONAL)

LEGEND

EOT	END OF TRANSMISSION	CR	CARRIAGE RETURN
LF	LINE FEED	DC1	STANDARD CODE FOR SERIAL PRINT TO PLOT MODE CHANGE
FF	FORM FEED		

NOTE: EMPTY SPACES ARE UNASSIGNED AND IGNORED.

*optional codes for serial print/plot mode change.

**These two columns not used with 124 character set.

FIGURE 8. VERSATEC CHARACTER SETS

Serial inputs may be applied at rates from 110 to 9600 BPS synchronous by bit and asynchronous by character or byte. Each character or byte consists of 10 or 11 elements as shown in Figure 7. The first bit is the start bit which causes the clock in the printer to start and run at a predetermined rate. The rate is determined by the placement of a jumper wire on the Input Logic PC board. The rate can be set for 9600, 4800, 2400, 1200, 600, 300, 150, and 110 BPS. The maximum rate is 19,200 BPS on 2030 and 1110A models. The next eight bits contain the data code. The character code accepted for print data is ASCII. Plotting data are unweighted binary. The stop bits are ignored. Printing operations are as described earlier, except that remote control lines are not used. The print mode of operation is normally selected. Plotting mode may be selected by entering an ASCII control character, DC1, 021 (OCTAL). This control code must be transmitted as the first byte preceding plotting data. At the completion of the scan, the Versatec unit reverts to the printing mode. Printing or plotting at very slow rates may cause poor print quality due to overdevelopment of the image. Therefore, printing serially at low rates, below 600 BPS, is not recommended. Likewise, plotting serially at less than 2400 BPS is not recommended.

CONTROLLERS FOR OPERATING VERSATEC UNITS

Versatec controllers are available for the computers listed below. For complete specifications on each model, refer to the separate Versatec data sheets on controllers. Controllers and special interface designs for other equipment will be quoted on request.

- Data General NOVA and Super NOVA series.
- Digital Equipment Corporation PDP8, PDP11, PDP12, and PDP9/15.
- Hewlett-Packard 2100, 2114, 2115, 2116, 2100A, 2100S, 21MX.
- Varian 620 and 73.
- Xerox Data Systems Sigma series.
- Honeywell 316 and 516.
- Interdata 70, 74, 80, 85, 6/16, 7/16, 7/32 and 8/32.
- IBM 360, 370, 1130.
- Digital Computer Controls D116 series.
- ROLM computers.

LONG LINE DRIVERS AND RECEIVERS (See Figure 9)

Differential line drivers and receivers are used in both controllers and Versatec units to enable long line communications. The interface cables may be twisted (#24-gauge stranded wire) cable. The Versatec I/O circuits for cable lengths greater than 50 feet but less than 1500 feet are shown in Figure 10.

The signals which are not differentially activated are ONLIN and NOPAP. The driver for these signals is a TTL 7437 buffer circuit for which the controller receiver is a resistor terminator network and TTL load.

The schematic below describes the typical input and output circuits provided by Versatec electrostatic units. Input signals are applied to a typical receiver. Output signals are driven from a typical driver. Interface cables are limited to 50 feet in length, twisted pair, two twists per inch, #24 gauge stranded wire.

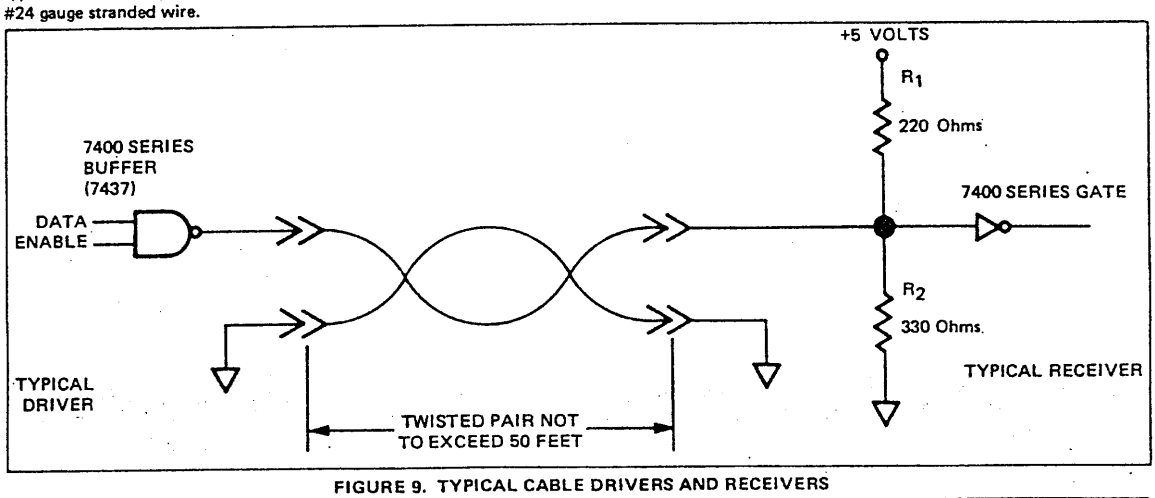


FIGURE 9. TYPICAL CABLE DRIVERS AND RECEIVERS

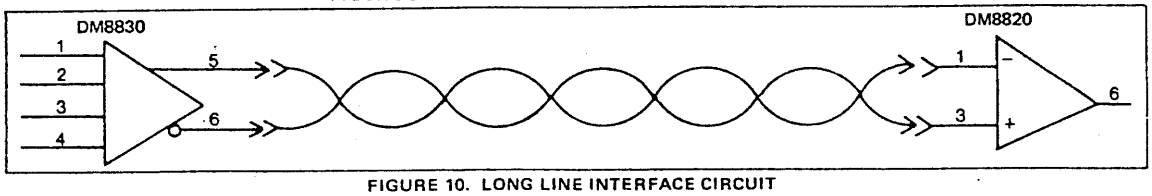


FIGURE 10. LONG LINE INTERFACE CIRCUIT

VERSATEC
A XEROX COMPANY
2805 Bowers Avenue
Santa Clara, California 95051
(408) 988-2800
TWX: 910-338-0243

datalog
Rygårds Allé 104
2900 Hellerup
Tlf. 01 - 20 00 66.

Bulletin No. 312, September 1977 Printed in U.S.A.

VIÐAUKI B.

ASYNCHRONOUS FIFO INTERFACE HP 2711A

Table 3-2. Pinout of Wire Wrap Connector for Differential Cable 27114-63001 and 27114-63003 (1 of 3)

WIRE WRAP PINOUT	DEVICE ADAPTER PINOUT	SIGNAL MNEMONIC	SIGNAL DEFINITION (As seen by host)*
A1	B1	SD0-	Data Bit 0 Low True SEND
A2	B4		Reserved for future use
A3	B3	SD1-	Data Bit 1 Low True SEND
A4	B2		Reserved for future use
A5	C6	SD2-	Data Bit 2 Low True SEND
A6	B8		Reserved for future use
A7	B7	SD3-	Data Bit 3 Low True SEND
A8	B6		Reserved for future use
A9	C10	SD4-	Data Bit 4 Low True SEND
A10	A10	SHIELD	Frame Ground
A11	B11	SD5-	Data Bit 5 Low True SEND
A12	B32	PDIR+	DIRECTION High True SEND
A13	C14	SD6-	Data Bit 6 Low True SEND
A14	A22	PCTL-	PCTL Low True SEND
A15	B15	SD7-	Data Bit 7 Low True SEND
A16	A24	CTL0+	CONTROL 0 High True SEND
A17	B17	SD8+	Data Bit 8 High True SEND
A18	B26	CTL1-	CONTROL 1 Low True SEND
A19	C21	SD9+	Data Bit 9 High True SEND
A20	B20	GND	Signal Ground
A21	C19	RD9-	Data Bit 9 Low True RECEIVE
A22	A14	PFLG-	PFLAG Low True RECEIVE
A23	B23	SD11-	Data Bit 11 High True SEND
A24	A16	STS0+	STATUS 0 High True RECEIVE
A25	B25	SD12-	Data Bit 12 High True SEND
A26	B18	STS1+	STATUS 1 High True RECEIVE
A27	C28	SD13+	Data Bit 13 High True SEND
A28	B30	ATTN-	ATTENTION Low True RECEIVE
A29	B29	SD14+	Data Bit 14 High True SEND
A30	B28	CTL2+	CONTROL 2 High True SEND
A31	C32	SD15+	Data Bit 15 High True SEND
A32			Reserved for future use
	B12		Reserved for future use

*EXAMPLE:
SEND = Connected to host driver
RECEIVE = Connected to host receiver

Table 3-2. Pinout of Wire Wrap Connector for Differential Cable 27114-63001 and 27114-63003 (2 of 3)

WIRE WRAP PINOUT	DEVICE ADAPTER PINOUT	SIGNAL MNEMONIC	SIGNAL DEFINITION (As seen by host)*
B1	A1	RD0-	Data Bit 0 Low True RECEIVE
B2	A4		Reserved for future use
B3	A3	RD1-	Data Bit 1 Low True RECEIVE
B4	A2		Reserved for future use
B5	C5	RD2+	Data Bit 2 High True RECEIVE
B6	A8		Reserved for future use
B7	A7	RD3-	Data Bit 3 Low True RECEIVE
B8	A6		Reserved for future use
B9	C9	RD4+	Data Bit 4 High True RECEIVE
B10			Not used
	B10	TEST	
B11	A11	RD5-	Data Bit 5 Low True RECEIVE
B12	B12	PDIR-	DIRECTION Low True SEND
B13	C13	RD6+	Data Bit 6 High True RECEIVE
B14	B22	PCTL+	PCTL High True SEND
B15	A15	RD7-	Data Bit 7 Low True RECEIVE
B16	B24	CTL0-	CONTROL 0 Low True SEND
B17	A17	RD8+	Data Bit 8 High True RECEIVE
B18	A26	CTL1+	CONTROL 1 High True SEND
B19	C22	SD10-	Data Bit 10 Low True SEND
B20	A20	GND	Signal Ground
B21	C20	RD10+	Data Bit 10 High True RECEIVE
B22	B14	PFLG+	PFLAG High True RECEIVE
B23	A23	RD11+	Data Bit 11 High True RECEIVE
B24	B16	STS0-	STATUS 0 Low True RECEIVE
B25	A25	RD12+	Data Bit 12 High True RECEIVE
B26	A18	STS1-	STATUS 1 Low True RECEIVE
B27	C27	RD13-	Data Bit 13 Low True RECEIVE
B28	A30	ATTN+	ATTENTION High True RECEIVE
B29	A29	RD14+	Data Bit 14 High True RECEIVE
B30	A28	CTL2-	CONTROL 2 Low True SEND
B31	C31	RD15-	Data Bit 15 Low True RECEIVE
B32			Reserved for future use
	A12		Reserved for future use

*EXAMPLE:
SEND = Connected to host driver
RECEIVE = Connected to host receiver

Table 3-2. Pinout of Wire Wrap Connector for Differential Cable 27114-63001 and 27114-63003 (3 of 3)

WIRE WRAP PINOUT	DEVICE ADAPTER PINOUT	SIGNAL MNEMONIC	SIGNAL DEFINITION (As seen by host)*			
C1	C2	SD0+	Data Bit	0	High True	SEND
C2	C1	RD0+	Data Bit	0	High True	RECEIVE
C3	C4	SD1+	Data Bit	1	High True	SEND
C4	C3	RD1+	Data Bit	1	High True	RECEIVE
C5	B5	SD2+	Data Bit	2	High True	SEND
C6	A5	RD2-	Data Bit	2	Low True	RECEIVE
C7	C8	SD3+	Data Bit	3	High True	SEND
C8	C7	RD3+	Data Bit	3	High True	RECEIVE
C9	B9	SD4+	Data Bit	4	High True	SEND
C10	A9	RD4-	Data Bit	4	Low True	RECEIVE
C11	C12	SD5+	Data Bit	5	High True	SEND
C12	C11	RD5+	Data Bit	5	High True	RECEIVE
C13	B13	SD6+	Data Bit	6	High True	SEND
C14	A13	RD6-	Data Bit	6	Low True	RECEIVE
C15	C16	SD7+	Data Bit	7	High True	SEND
C16	C15	RD7+	Data Bit	7	High True	RECEIVE
C17	C18	SD8-	Data Bit	8	Low True	SEND
C18	C17	RD8-	Data Bit	8	Low True	RECEIVE
C19	A21	SD9-	Data Bit	9	Low True	SEND
C20	B21	SD10+	Data Bit	10	High True	SEND
C21	A19	RD9+	Data Bit	9	High True	RECEIVE
C22	B19	RD10-	Data Bit	10	Low True	RECEIVE
C23	C24	SD11-	Data Bit	11	Low True	SEND
C24	C23	RD11-	Data Bit	11	Low True	RECEIVE
C25	C25	SD12-	Data Bit	12	Low True	SEND
C26	C26	RD12-	Data Bit	12	Low True	RECEIVE
C27	B27	SD13-	Data Bit	13	Low True	SEND
C28	A27	RD13+	Data Bit	13	High True	RECEIVE
C29	C30	SD14-	Data Bit	14	Low True	SEND
C30	C29	RD14-	Data Bit	14	Low True	RECEIVE
C31	B31	SD15-	Data Bit	15	Low True	SEND
C32	A31	RD15+	Data Bit	15	High True	RECEIVE

*EXAMPLE:
SEND = Connected to host driver
RECEIVE = Connected to host receiver

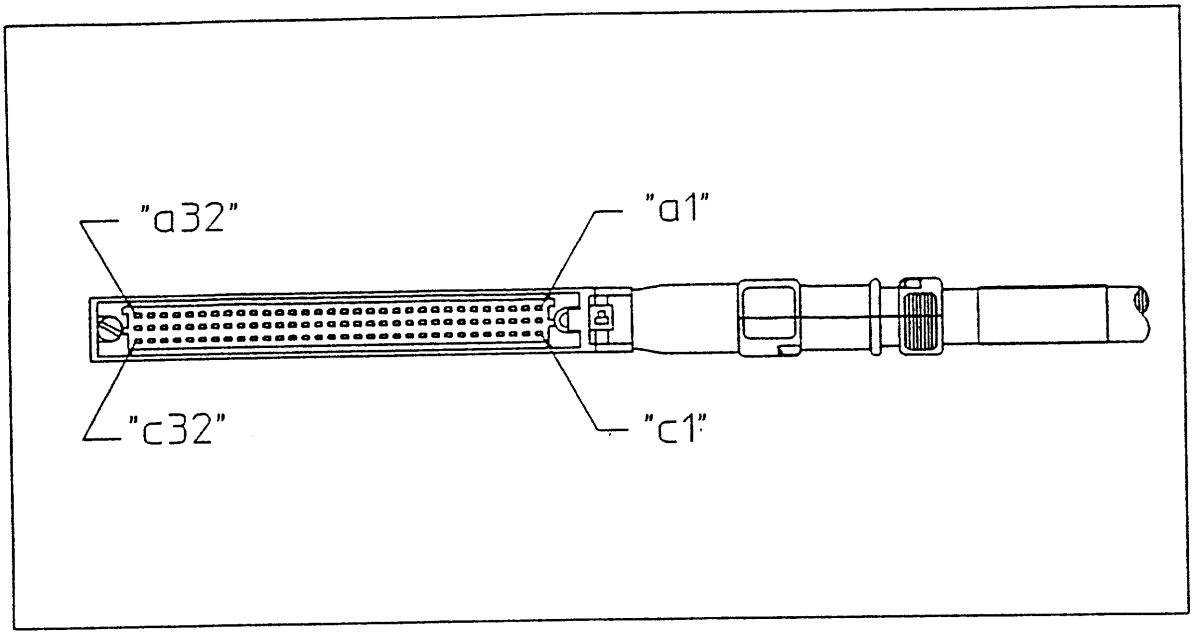


Figure 3-1. Wire Wrap Pinout Orientation

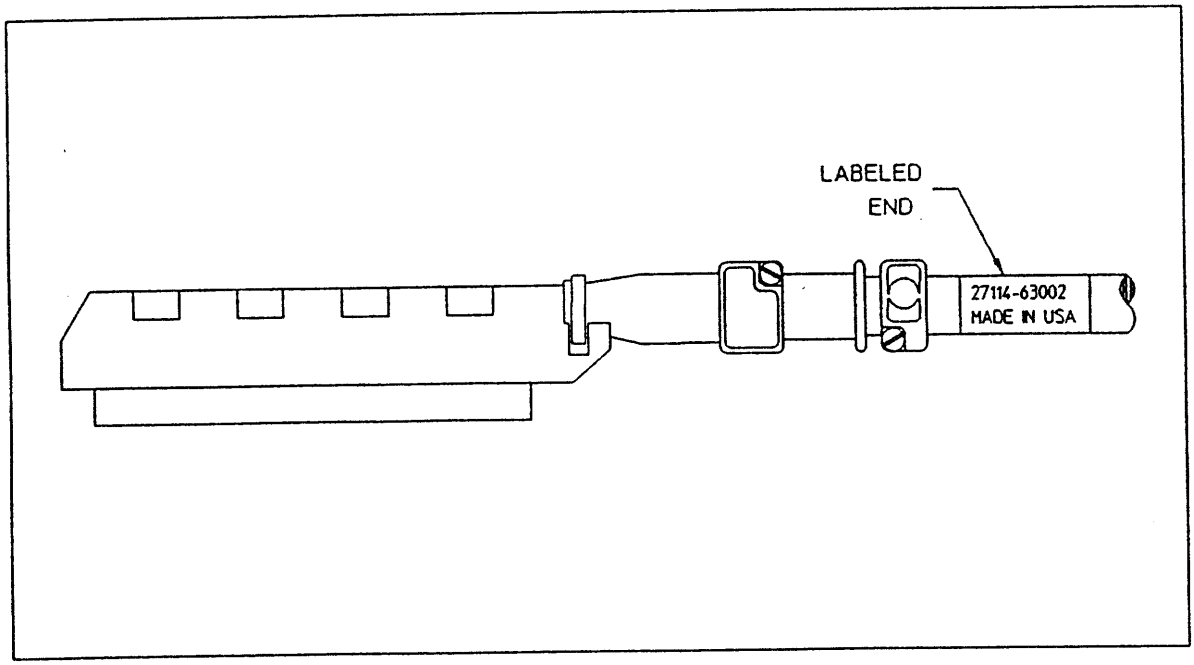


Figure 3-2. 27114-63002 Cable Connector